Fibocom
PERFECT WIRELESS EXPERIENCE

# FG132
# Hardware Guide

V1.4

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# Contents

# Applicable Models

| No. | Applicable Model | Description |
|---|---|---|
| 1 | FG132-GL-00 | 5G Redcap, 2Gb FLASH, 2Gb DDR2, GL band, MAIN+DIV and GNSS ANT, 5G/4G |
| 2 | FG132-CN-00 | 5G Redcap, 2Gb FLASH, 2Gb DDR2, CN band, MAIN+DIV and GNSS ANT, 5G/4G |
| 3 | FG132-NA-00 | 5G Redcap, 2Gb FLASH, 2Gb DDR2, NA band, MAIN+DIV and GNSS ANT, 5G/4G |
| 4 | FG132-EAU-00 | 5G Redcap, 2Gb FLASH, 2Gb DDR2, EAU band, MAIN+DIV and GNSS ANT, 5G/4G |
| 5 | FG132-NA-30 | 5G Redcap, 4Gb FLASH, 2Gb DDR2, NA band, MAIN+DIV and GNSS ANT, 5G/4G |

# Change History

| | |
|---|---|
| V1.4 (2024-9-11) | Chapter 6.2, Update power consumption data<br>Chapter 3.1, Update pin map |
| V1.3 (2024-7-11) | Chapter 2, Add NA-30 type |
| V1.2 (2024-6-20) | Chapter 2, Add EAU type<br>Chapter 7.3, Add PCB package pattern |
| V1.1 (2024-4-24) | Chapter 2, Add CN and NA type. |
| V1.0 (2023-10-23) | First version. |
| Draft (2023-9-12) | Draft version. |

# 1 Foreword

## 1.1 Description

This document describes information on electrical characteristics, RF performance, structural dimensions and application environment of the FG132 series module. With the help of this document and other related documents, the application developer can quickly understand the hardware functions of the module and develop the hardware of the product.

## 1.2 Reference Standards

This product is designed with reference to the following standards:

- 3GPP TS 36.521-1 V15.0.0: User Equipment (UE) conformance specification; Radio transmission and reception; Part 1: Conformance testing
- 3GPP TS 36.124V10.3.0: Electro Magnetic Compatibility (EMC) requirements for mobile terminals and ancillary equipment
- 3GPP TS 21.111 V10.0.0: USIM and IC card requirements
- 3GPP TS 51.011 V4.15.0：Specification of the Subscriber Identity Module -Mobile Equipment (SIM-ME) interface
- 3GPP TS 31.102 V10.11.0：Characteristics of the Universal Subscriber Identity Module (USIM) application
- 3GPP TS 31.11 V10.16.0: Universal Subscriber Identity Module (USIM) Application Toolkit (USAT)
- 3GPP TS 27.007 V10.0.8: AT command set for User Equipment (UE)
- 3GPP TS 27.005 V10.0.1: Use of Data Terminal Equipment -Data Circuit terminating Equipment (DTE – DCE) interface for Short Message Service (SMS) and Cell Broadcast Service （CBS）38521-1-i00（NR; User Equipment (UE) conformance specification;
- Radio transmission and reception; Part 1 Range 1 standalone;
- Universal Serial Bus Specification 2.0

# 2 Product Overview

## 2.1 Product Introduction

FG132 series products are packaged in LGA, which is a highly integrated 5G wireless communication module and supports LTE-FDD/LTE-TDD network modes. The module can provide stable and high-speed data transmission services, suitable for most mobile operator networks around the world, and can be used in IPC and Industrial gateway applications, etc.

Table 1. Band introduction

| Model | Number of Antennas | Network Type | Band Configuration |
|---|---|---|---|
| FG132-GL-00 | 3 | 5G NR | SA: n1/2/3/5/7/8/12/13/14/18/20/25/26/28/30/38/40/41/48/66/70/71/77/78 |
| | | LTE | LTE: B1/2/3/4/5/7/8/12/13/14/17/18/19/20/25/26/28/30/34/38/39/40/41/42/43/48/66/71 |
| | | GNSS | GPS/GLONASS/BDS/Galileo/ QZSS |
| FG132-CN-00 | 3 | 5G NR | SA: n1/3/5/8/28/40/41/78/79 |
| | | LTE | LTE: B1/3/5/8/34/38/39/40/41 |
| | | GNSS | GPS/GLONASS/BDS/Galileo/QZSS |
| FG132-NA-00/30 | 3 | 5G NR | SA: n2/5/7/12/13/14/25/26/30/38/41/48/66/70/71/77/78 |
| | | LTE | LTE: B2/4/5/7/12/13/14/17/25/26/30/38/41/42/43/48/66/71 |
| | | GNSS | GPS/GLONASS/BDS/Galileo/QZSS |
| FG132-EAU-00 | 3 | 5G NR | SA: n1/3/5/7/8/20/28/38/40/41/77/78 |
| | | LTE | LTE: B1/3/5/7/8/20/28/38/40/41/42/43 |
| | | GNSS | GPS/GLONASS/BDS/Galileo/QZSS |

## 2.2 Key Features

Table 2. Key features

| Category | Function Description |
|---|---|
| Power supply | DC: 3.3V–4.3V, typical voltage: 3.8V |

| | |
|---|---|
| PC operating system | Linux/Windows/Android |
| Network protocol | 3GPP Release 17 |
| SMS | Supported |
| Storage configuration | 2Gb DDR2+2Gb or 4Gb NAND Flash |
| Function interface | USB×1: USB2.0, Used for AT command communication, data transmission, software debugging and firmware upgrade |
| | I2C×1: Only support master mode, support 100KHz and 400KHz baud rate |
| | SPI×1: Only support standard SPI interface, CLK frequency up to 50MHz |
| | ADCx2: Voltage range is 0~VBAT_BB |
| | UART×3: Main UART: Used for AT command communication and data transmission; Baud rates reach up to 4Mbps, 115200 bps by default; Support RTS and CTS hardware flow control, disabled by default and need software enable. When the baud rate is above 1Mbps, it is recommended to use hardware flow control.<br>Debug UART: Used for Linux console and log output; 115200bps baud rate.<br>Coex UART: Only used for 5G/LTE and WLAN coexist |
| | SGMII×1: Support 10 Mbps/100 Mbps/1000 Mbps Ethernet work mode |
| | SIM×2: Support 1.8V and 3V SIM Card, Support hot plug |
| | PCMx1: Used for audio function with external codec; Support 16-bit linear data format; Support long frame synchronization and short frame synchronization; Support master and slave* modes |
| | PCIEx1: Complaint with PCIe Gen 2,1 lane; Support RC and EP* mode |
| Antenna | MAIN Antenna<br>DIV Antenna<br>GNSS Antenna |
| LTE features | UL supports QPSK, 16QAM and 64QAM modulations<br>DL supports QPSK, 16QAM, 64QAM and 256QAM modulations<br>A maximum uplink rate of 75Mbps and a maximum downlink rate of 195Mbps |
| 5G NR features | UL supports QPSK, 16QAM, 64QAM, 256QAM and PI/2 BPSK modulations<br>DL supports QPSK, 16QAM, 64QAM and 256QAM modulations<br>A maximum uplink rate of 123 Mbps and a maximum downlink rate of 223 Mbps |
| RF Power level | 5G NR Band: Class 3 (23 dBm ±2 dB)<br>LTE Band: Class 3 (23 dBm ±2 dB)<br>LTE HPUE Band: Class 2 (26 dBm ±2 dB) |

| | |
|---|---|
| 5G SRS | Support 1T2R (n38/40/41/48/77/78/79) |
| GNSS features | Supports dual-band GNSS: L1/L5<br>Supports GPS, GLONASS, BDS, Galileo/ QZSS<br>Supports Gen 9 v5.1 engine<br>Protocol: NMEA 0183<br>Data update rate: 1 Hz by default |
| Physical features | Dimensions: (32.0±0.15) mm × (29.0±0.15) mm × (2.4±0.2) mm<br>Package: LGA<br>Weight: 5.3g±0.5g |
| Temperature features | Operating temperature: -35°C to +75°C,<br>Expansion temperature: -40°C to +85°C, When the ambient temperature is within the range of -35~-40°C at low temperatures and 75~85°C at high temperatures, some indexes may exceed 3GPP standard<br>Storage temperature: –45°C to +90°C |
| Software upgrade | Through USB/FOTA |

# 2.3 Hardware Block Diagram

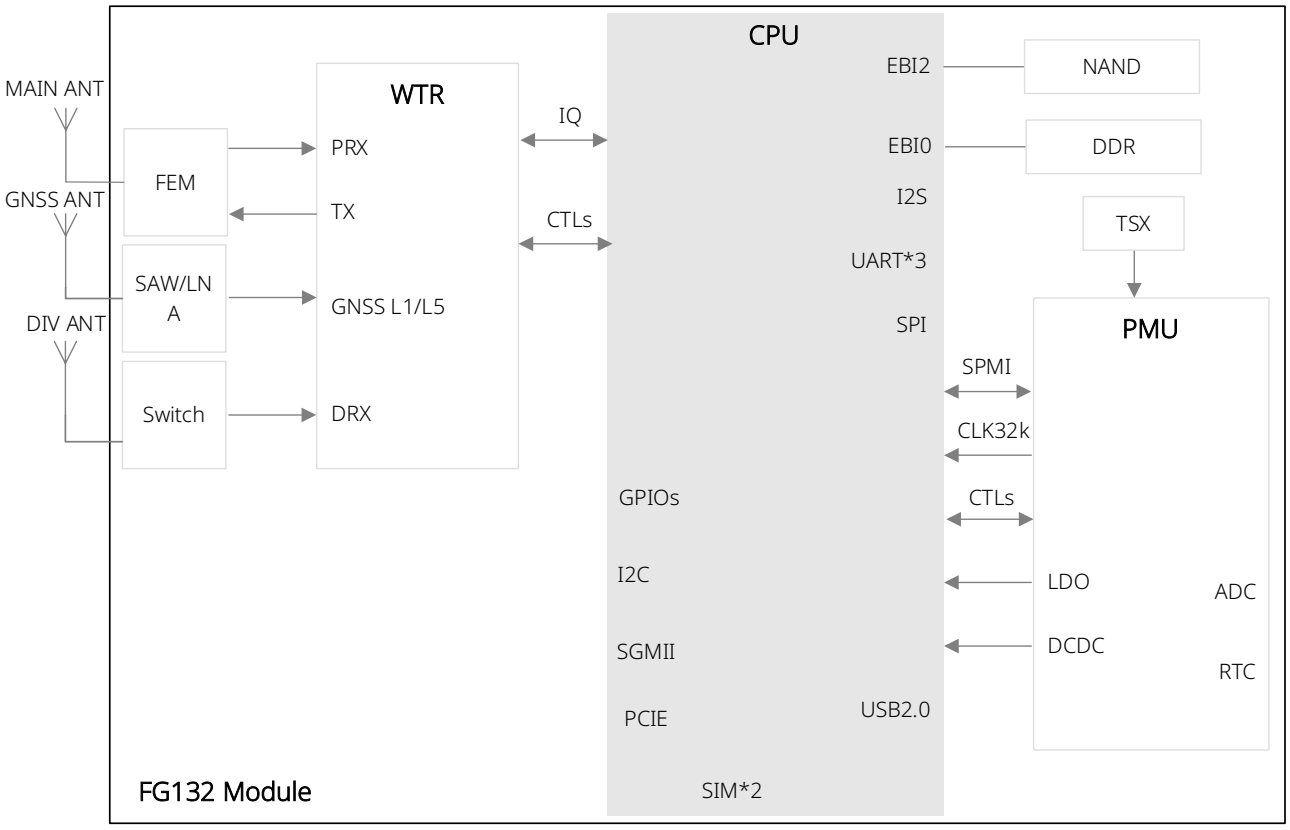



Figure 1. Hardware block diagram

The above figure is the hardware block diagram of the module, which mainly introduces the key components and functions of the baseband and RF parts.

- PMU: power management chip.
- CPU: which is mainly responsible for processing instructions, executing operations, controlling time, processing data and other functions.
- MCP: DDR2 and NAND Flash memory, which combines the high density of EPROM with the flexibility of EEPROM structure to hold data after power failure.
- WTR: RF transceiver IC, which supports 5G NR.
- FEM: Front-end Modules

## 2.4 Description of Development Kit

Fibocom configures a complete development board kit for the module, which makes it convenient for users to quickly understand the module performance. Refer to *Fibocom_ADP-FG132_Development Board User Guide* and *Fibocom_EVB-LGA-F01_User Guide* for the usage of development board.

The EVK-LGA-F01 development board can support the development and testing needs of WI-FI and Ethernet usage scenarios, while the ADP development board can meet the development and testing needs of all other usage scenarios, include: USB/UART/LCD/SIM/CODEC/Antenna/key/power supply, etc.

# 3 Pin Definition

## 3.1 Pin Distribution

The FG132 series modules are in LGA package, with a total of 204 pins. The following figure is a TOP perspective view.

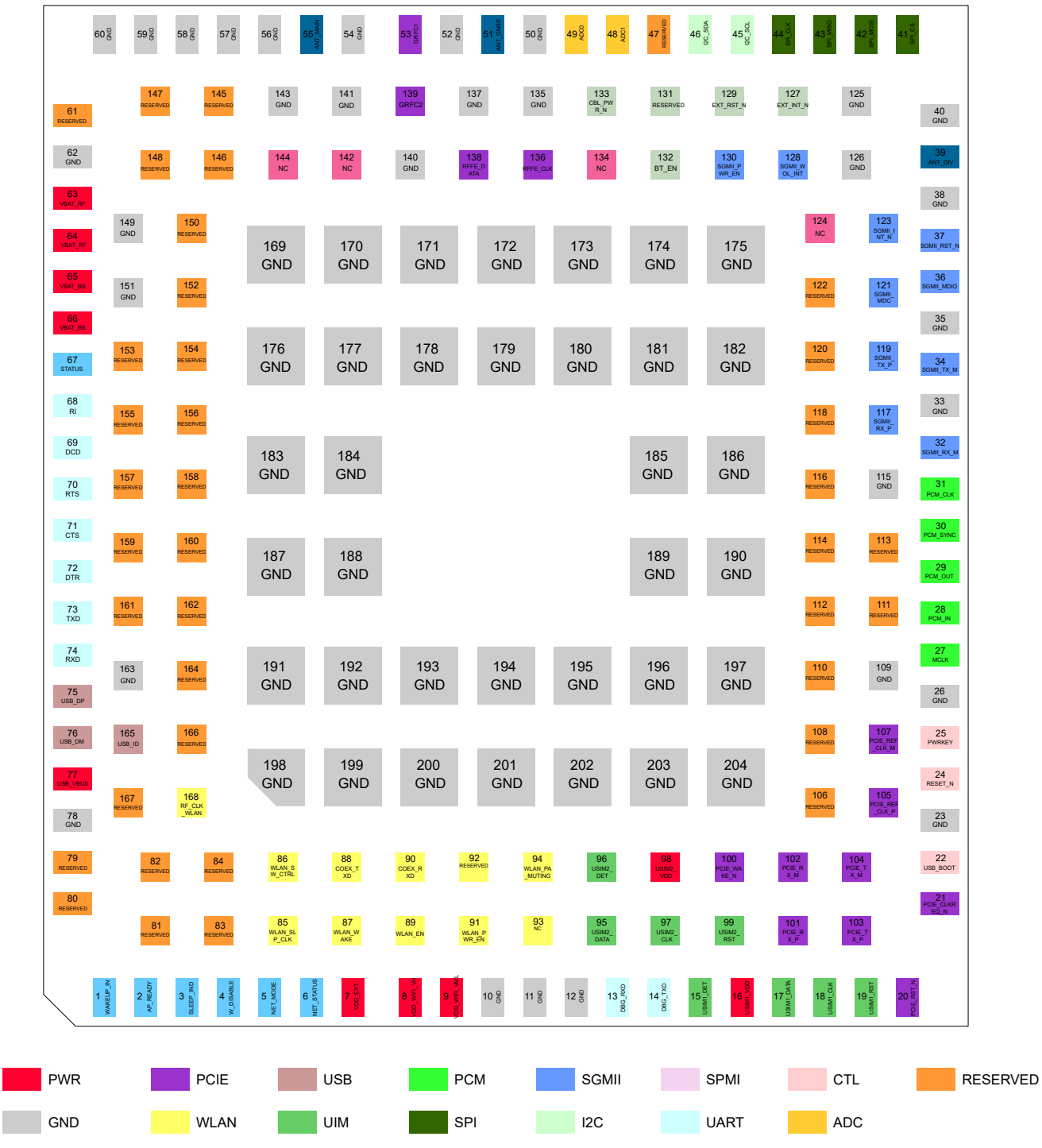



Figure 2. Pin distribution

# 3.2 Pin Description

Table 3. I/O type definition

| Type | Description | Type | Description |
|---|---|---|---|
| PI | Power input | AIO | Analog input and output |
| PO | Power output | OD | Open drain |
| DI | Digital input | PU | Pull-up high level |
| DO | Digital output | PD | Pull-down low level |
| DIO | Digital input and output | T | Tristate, that is, high resistance state, which is determined by the peripheral circuit |
| AI | Analog input | G | Ground |
| AO | Analog output | NP | No pull |
| Unstable | The voltage level is unstable, and the software is uncontrollable for a period of time after power on. The waveform is unstable, and it is not recommended to connect devices that are sensitive to the voltage level | | |

Table 4. Power interfaces

| Pin | Pin Name | I/O | Reset Value[1] | Pin Description | DC Feature |
|---|---|---|---|---|---|
| 7 | VDD_EXT | PO | - - | 1.8V power output, 50mA current capable | 1.8V |
| 16 | USIM1_VDD | PO | - - | USIM1 power output | 1.8V/2.95V |
| 98 | USIM2_VDD | PO | - - | USIM2 power output | 1.8V/2.95V |
| 8 | VDD_WIFI_VH | PO | - - | WIFI power output | 1.95V |
| 9 | VDD_WIFI_VML | PO | - - | WIFI power output | 1.35V |
| 63 | VBAT_RF | PI | - - | RF power input | 3.3V~4.3V, typical 3.8V, 2.6A current need |
| 64 | VBAT_RF | PI | - - | RF power input | |
| 65 | VBAT_BB | PI | - - | Baseband power input | |
| 66 | VBAT_BB | PI | - - | Baseband power input | |
| 10~12, 23, 26, 33, 35, 38, 40, 50, 52, 54, 56~60, 62, 78, 109, 115, 125, 126, 135, 137, 140, 141,143, 149, 151, 163, 169~204 | | | | | GND |

Table 5. Control interfaces

| Pin | Pin Name | I/O | Reset Value | Pin Description | DC Feature |
|---|---|---|---|---|---|
| 1 | WAKEUP_IN | DI | PD | Host trigger modules sleep or wake up, software can configure trigger levels | 1.8V |

| Pin | Pin Name | I/O | Reset Value | Pin Description | DC Feature |
|---|---|---|---|---|---|
| 4 | W_DISABLE# | DI | PD | Flight mode control signal, active low | 1.8V |
| 2 | AP_READY | DI | PD | Application processor sleep detection | 1.8V |
| 5 | NET_MODE | DO | PD | Module network mode indicator | 1.8V |
| 6 | NET_STATUS | DO | PD | Module network status indicator | 1.8V |
| 67 | STATUS | OD | Unstable | Module working status indicator | 1.8V |
| 3 | SLEEP_IND | DO | PD | Module sleep status output signal | 1.8V |
| 24 | RESET_N | DI | - - | Reset control signal, active low, pulled up internally | 1.5V |
| 25 | PWRKEY | DI | - - | Power on/off control signal, active low, pulled up internally | 1.5V |
| 133 | CBL_PWR_N | DI | - - | Auto power-on, active low; pulled up internally. | 0.8V |
| 22 | USB_BOOT | DI | - - | USB download mode boot signal, active high, must not be pulled up before startup.<br>A test point is recommended to reserve. | 1.8V |

Table 6. BB interfaces

| Pin | Pin Name | I/O | Reset Value | Pin Description | DC Feature |
|---|---|---|---|---|---|
| 15 | USIM1_DET | DI | PD | USIM1 card hot-plug detection, the function is turn on by default, active high | 1.8V |
| 17 | USIM1_DATA | DIO | Unstable | USIM1 data signal, add pull up 20k resistor external | 1.8V/2.95V |
| 18 | USIM1_CLK | DO | Unstable | USIM1 clock signal | 1.8V/2.95V |
| 19 | USIM1_RST | DO | Unstable | USIM1 reset signal | 1.8V/2.95V |
| 96 | USIM2_DET | DI | PD | USIM2 card hot-plug detection, the function is turn off by default, active high | 1.8V |
| 95 | USIM2_DATA | DIO | Unstable | USIM2 data signal, add pull up 20k resistor external | 1.8V/2.95V |
| 97 | USIM2_CLK | DO | Unstable | USIM2 clock signal | 1.8V/2.95V |
| 99 | USIM2_RST | DO | Unstable | USIM2 reset signal | 1.8V/2.95V |
| 27 | MCLK | DO | PD | I2S main clock output signal | 1.8V |

| Pin | Pin Name | I/O | Reset Value | Pin Description | DC Feature |
|---|---|---|---|---|---|
| 28 | PCM_DIN | DI | PD | PCM data transmission | 1.8V |
| 29 | PCM_DOUT | DO | PD | PCM data reception | 1.8V |
| 30 | PCM_SYNC | DIO | PD | PCM synchronization signal | 1.8V |
| 31 | PCM_CLK | DIO | PD | PCM clock signal | 1.8V |
| 41 | SPI_CS * | DI | PD | SPI chip selection signal | 1.8V |
| 42 | SPI_MOSI * | DO | PD | SPI data master output slave input | 1.8V |
| 43 | SPI_MISO * | DI | PD | SPI data slave output master input | 1.8V |
| 44 | SPI_CLK * | DO | PD | SPI clock signal | 1.8V |
| 45 | I2C_SCL | OD | Unstable | I2C clock signal, External pull-up resistor required | 1.8V |
| 46 | I2C_SDA | OD | PU | I2C data signal, External pull-up resistor required | 1.8V |
| 49 | ADC0 | AI | - - | Analog-to-digital input port 0 | 0~VBAT |
| 48 | ADC1 | AI | - - | Analog-to-digital input port 1 | 0~VBAT |
| 68 | RI | DO | PD | UART ringing prompt, reserved module wake-up host signal | 1.8V |
| 69 | DCD | DO | PD | UART output carrier detection signal, reserved | 1.8V |
| 70 | RTS | DO | PD | UART request to send signal | 1.8V |
| 71 | CTS | DI | PD | UART clear to send signal | 1.8V |
| 72 | DTR | DI | PD | UART module wake-up, reserved host wake-up module signal | 1.8V |
| 73 | TXD | DO | PD | UART transmitting signal | 1.8V |
| 74 | RXD | DI | PD | UART receiving signal | 1.8V |
| 13 | DBG_RXD | DI | PD | Debug UART data reception, reserve test point | 1.8V |
| 14 | DBG_TXD | DO | Unstable | Debug UART data transmission, reserve test point | 1.8V |
| 75 | USB_DP | AIO | - - | USB 2.0 differential data signal (+) | - - |
| 76 | USB_DM | AIO | - - | USB 2.0 differential data signal (-) | - - |
| 77 | USB_VBUS | DI | - - | USB insertion detection | 3~5.25V, typical 5V |
| 37 | SGMII_RST_N | DO | Unstable | SGMII reset output for external PHY | 1.8V |

| Pin | Pin Name | I/O | Reset Value | Pin Description | DC Feature |
|---|---|---|---|---|---|
| 123 | SGMII_INT_N | DI | PD | SGMII interrupt | 1.8V |
| 128 | SGMII_WOL_INT_N | DI | PD | SGMII wake-on-LAN interrupt | 1.8V |
| 130 | SGMII_PWR_EN | DO | Unstable | SGMII external power enable | 1.8V |
| 121 | SGMII_MDC | DO | Unstable | SGMII management Data Input/Output clock | 1.8V |
| 36 | SGMII_MDIO | DIO | Unstable | SGMII management Data Input/Output data | 1.8V |
| 34 | SGMII_TX_M | AO | - - | SGMII transmission (-) | - - |
| 119 | SGMII_TX_P | AO | - - | SGMII transmission (+) | - - |
| 32 | SGMII_RX_M | AI | - - | SGMII receive (-), Connect with a 0.1μF capacitor, and be close to the PHY side | - - |
| 117 | SGMII_RX_P | AI | - - | SGMII receive (+), Connect with a 0.1μF capacitor, and be close to the PHY side | - - |
| 105 | PCIe_REFCLK_P | AIO | - - | Positive end of PCIe reference clock signal. | - - |
| 107 | PCIe_REFCLK_M | AIO | - - | Negative end of PCIe reference clock signal. | - - |
| 103 | PCIe_TX_P | AO | - - | Positive end of PCIe data transmitting signal | - - |
| 104 | PCIe_TX_M | AO | - - | Negative end of PCIe data transmitting signal | - - |
| 101 | PCIe_RX_P | AI | - - | Positive end of PCIe data receiving signal. Connect with a 0.22μF capacitor, and be close to the WIFI side | - - |
| 102 | PCIe_RX_M | AI | - - | Negative end of PCIe data receiving signal. Connect with a 0.22μF capacitor, and be close to the WIFI side | - - |
| 20 | PCIe_RST_N | DIO | Unstable | PCIe reset signal | 1.8V |
| 21 | PCIe_CLKREQ_N | OD/DIO | Unstable | PCIe clock request signal | 1.8V |
| 100 | PCIe_WAKE_N | OD/DIO | PU | PCIe wake-up signal | 1.8V |
| 127 | EXT_INT_N * | DI | PD | External audio interruption | 1.8V |
| 129 | EXT_RST_N * | DO | PD | External audio reset | 1.8V |

| Pin | Pin Name | I/O | Reset Value | Pin Description | DC Feature |
|---|---|---|---|---|---|
| 165 | USB_ID * | DI | PD | USB OTG | 1.8V |

Table 7. Tuner interfaces

| Pin | Pin Name | I/O | Reset Value | Pin Description | DC Feature |
|---|---|---|---|---|---|
| 39 | ANT_DIV | AI | - - | DIV Antenna | - - |
| 55 | ANT_MAIN | AIO | - - | MAIN Antenna | - - |
| 51 | ANT_GNSS | AI | - - | GNSS Antenna | - - |
| 53 | GRFC1 | DO | PD | Generic RF Controller1 | 1.8V |
| 139 | GRFC2 | DO | PD | Generic RF Controller2 | 1.8V |
| 138 | RFFE_DATA | DIO | PD | RFFE data signal | 1.8V |
| 136 | RFFE_CLK | DO | PD | RFFE clock signal | 1.8V |

Table 8. WLAN/BT control interfaces

| Pin | Pin Name | I/O | Reset Value | Pin Description | DC Feature |
|---|---|---|---|---|---|
| 91 | WLAN_PWR_EN | DO | PD | WLAN power supply enable control | 1.8V |
| 87 | WLAN_WAKE | DI | PD | WLAN wake-up module | 1.8V |
| 89 | WLAN_EN | DO | Unstable | WLAN enable control | 1.8V |
| 132 | BT_EN | DO | PD | BT enable control | 1.8V |
| 94 | WLAN_PA_MUTING | DO | PU | To disable WLAN 2.4GHz chain 1PA | 1.8V |
| 86 | WLAN_SW_CTRL | DI | PD | WIFI VDD_FEM Power control | 1.8V |
| 90 | COEX_UART_RXD | DI | PD | 5G/LTE and WLAN coexistence receive | 1.8V |
| 88 | COEX_UART_TXD | DO | PD | 5G/LTE and WLAN coexistence transmit | 1.8V |
| 85 | WLAN_SLP_CLK | DO | Unstable | WLAN sleep clock | 1.8V |
| 168 | RF_CLK_WLAN | DO | - - | WLAN main clock | 1.8V |

Table 9. NC & Reserved interfaces

| Pin | Pin Description |
|---|---|
| 47, 61, 79~84, 92, 106, 108, 110~114, 116, 118, 120, 122, 131, 145~148, 150, 152~162, 164, 166, 167 | Reserved |
| 93, 124, 134, 142, 144 | NC |

- Reset Value: The state during pin initialization.
- Pins marked with "*" are reserved or under development.
- pin22, 108, 147, 154~156, 159~162, 164 and 166 should not pull up during module initialization stage.
- CN type support the n79 band, so pin92 and pin93 to reserve coexistence.

# 4 Application Interfaces

## 4.1 Power Interfaces

Table 10. Electrical Parameter

| Parameter | | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| Power supply | VBAT | 3.3 | 3.8 | 4.3 | V |
| | VBUS | 3 | 5 | 5.25 | V |

Table 11. Absolute Maximum Ratings

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| Power supply | VBAT | -0.3 | 4.7 | V |
| | VBUS | -0.3 | 5.25 | V |
| Analog level | ADC | 0 | VBAT_BB | V |
| Digital level | GPIO | -0.5 | 2.2 | V |

### 4.1.1 Power Supply Circuit

The power supply of the module ranges from 3.3V to 4.3V. You need to make sure that the input voltage is not lower than 3.3V.

To reduce voltage drop, two filter capacitors of 100μF with low ESR (ESR≤0.7Ω) are required. It is also recommended to reserve 5 chip multilayer ceramic capacitors (MLCC) with good ESR performance (22μF, 100nF, 6.8nF, 220pF, and 68pF) for VBAT_BB and 7 chip multilayer ceramic capacitors (MLCC) with good ESR performance (22μF, 100nF, 220pF, 68pF, 15pF, 9.1pF, and 4.7pF) for VBAT_RF, and the capacitors should be placed close to the VBAT pin. A star topology is required for VBAT_BB and VBAT_RF when an external power supply is connected to the module. The VBAT_BB trace width is not less than 1.5 mm, and the VBAT_RF trace width is not less than 2 mm. According to design rules, the longer the VBAT trace, the wider the trace width.

In addition, to suppress power fluctuations and shocks and ensure the stability of the output power supply, it is recommended to add a TVS array with a reverse operating voltage of 4.5V, low clamp voltage and high reverse pulse current at the front end of the power supply. The recommended model is ESDH4V5P1. The power star topology is shown in the following figure.

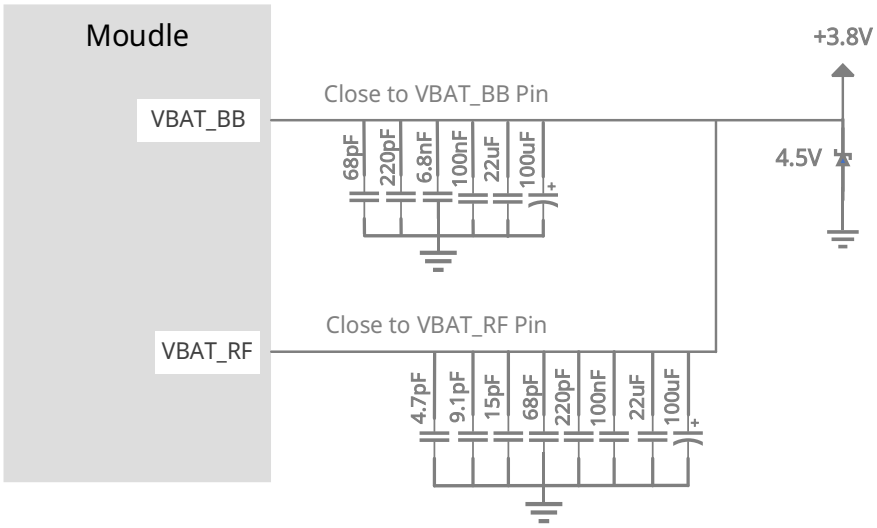



Figure 3. Power supply reference circuit

Filter capacitors should be placed close to the power supply pin, and the capacitance value should be smaller to be closer to the corresponding power supply pin. The filter capacitor is placed on the same side as the module, and must not cross the layer, otherwise there will be the risk of TIS interference, and the trace is as short and wide as possible.

The recommended filter capacitor can be adjusted by the customer based on specific circumstances. It is not a fixed value.

## 4.1.2 Voltage Drop

The customer should select a DC chip with a continuous output capability greater than 2.6A. The recommended input voltage for the module is 3.8V, with ripple less than 150mV. Add stabilizing capacitors to ensure that the VBAT voltage during module operation will not be continuously lower than 3.3V for more than 2ms, as it may trigger the shutdown mechanism of the module. The following figure shows the power supply requirements.

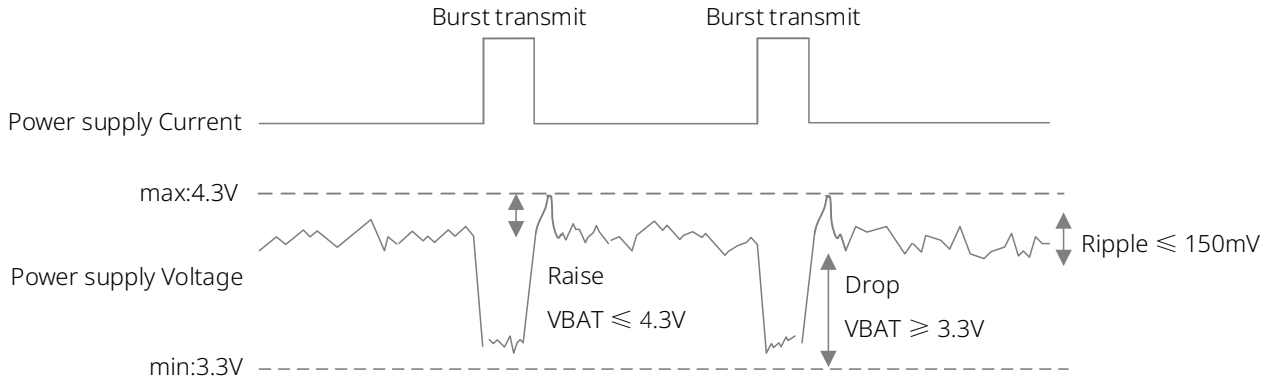



Figure 4. Power supply requirements

Due to the high peak current (about 2.6A) during the operation of the 5G module, the VBAT voltage fluctuation will gradually decrease with the increase of stabilizing capacitor, but it cannot be completely eliminated. Therefore, it is emphasized to customers that the power supply system of the module must be separated from the power supply of other control chips to avoid voltage fluctuations affecting the power stability of the control chip, leading to system shutdown.

## 4.2 Power-on/off Interfaces

When the module is in the power-off state, it can be powered on by pulling down the PWRKEY pin for 0.1s to 2s. The PWRKEY pin can be designed as a button to power on the module. To prevent electrostatic impact caused by contact, a TVS tube needs to be placed near the button for ESD protection. The button switch circuit is as follows:

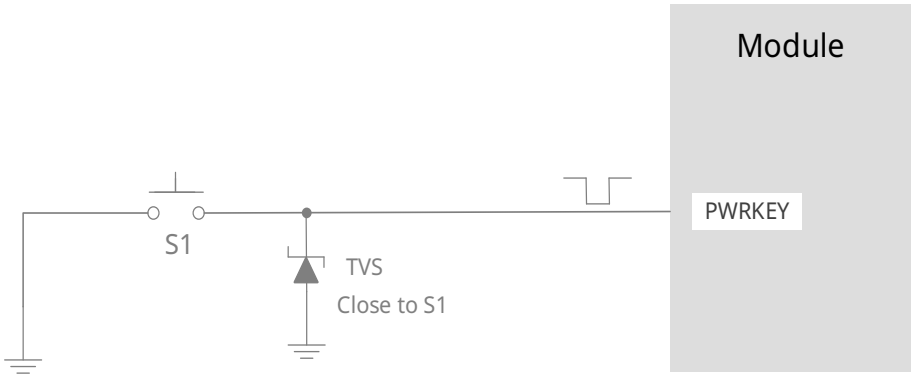



Figure 5. PWRKEY button switch circuit

It is recommended to use an OC or OD drive circuit to control PWRKEY. The power on/off circuit is shown in the following figure.

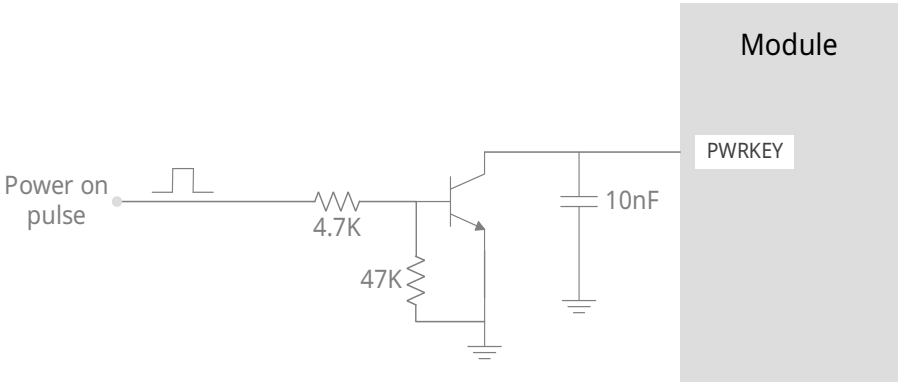



Figure 6. OC drive power on/off circuit

After the module is powered on and initialized, the pin defaults to 1.5V high level, which does not require

external pull-up. The module power-on process is as follows:

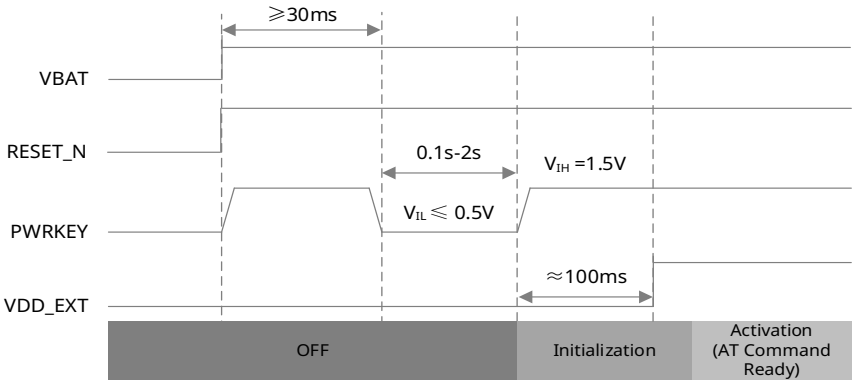



Figure 7. Power-on timing sequence

When the module is in the powered-on state, there are two ways to initiate the power-off process. They are as follows:

- Pulling down the PWRKEY pin for 3s to 8s and then releasing it will initiate the power-off process of the module. After releasing the PWRKEY signal, there should be a minimum interval of 25 seconds before triggering the next power-on process. This time period is reserved for the module's power-off process.
- By sending the AT+CPWROFF command, you can initiate the soft power-off process of the module.

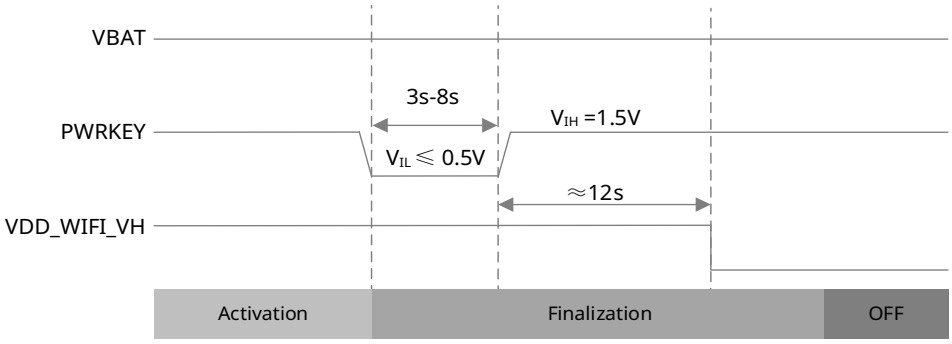



Figure 8. Power-off timing sequence

The module supports automatic power-on: connect the CBL_PWR_N pin in series with a 10kΩ resistor to GND, which allows the module to automatically power on when it is powered up.

The module with automatic power-on scheme cannot be power-off, only restarted. The circuit diagram is shown in the following figure.

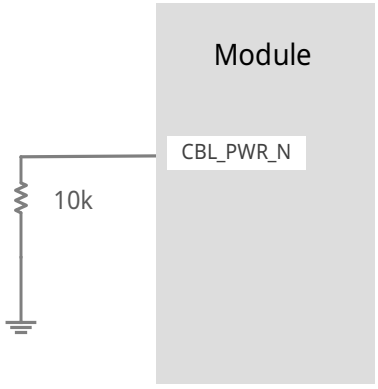



Figure 9. Automatic power-on circuit

- When the module is working properly, do not cut off the power supply of the module immediately to avoid damaging the internal flash. It is recommended to start the power-off process with AT command before disconnecting the power supply.
- Ensure VBAT voltage is stable before pulling down PWRKEY. It is recommended to pull down PWRKEY at least 30ms after VBAT is powered on and stable.
- When using AT command to power off the module, ensure PWRKEY is always in high level after the power-off command is executed, otherwise the module will be automatically powered on again after power-off.

## 4.3 Reset Interfaces

Table 12. Reset methods

| Reset Mode | Reset Method |
|---|---|
| Hardware reset | Pulling down the RESET pin for 700ms to 1s and then releasing it will initiate the reset process of the module. |
| Software reset | Sending the AT command AT+CFUN=15 will initiate the reset process of the module. |

The RESET pin of the module is set to high level by default after module initialization, so no external pull-up is required. When the RESET pin active low, the module is restarted. It is recommended to add a test point if not use. Reset signal is sensitive to interference, so it is recommended that module interface trace should be as short as possible, and it should be wrapped with ground. The reset reference circuit is similar to the PWRKEY control circuit and can be controlled using an OC or OD drive circuit or button. The circuit diagram is as follows:

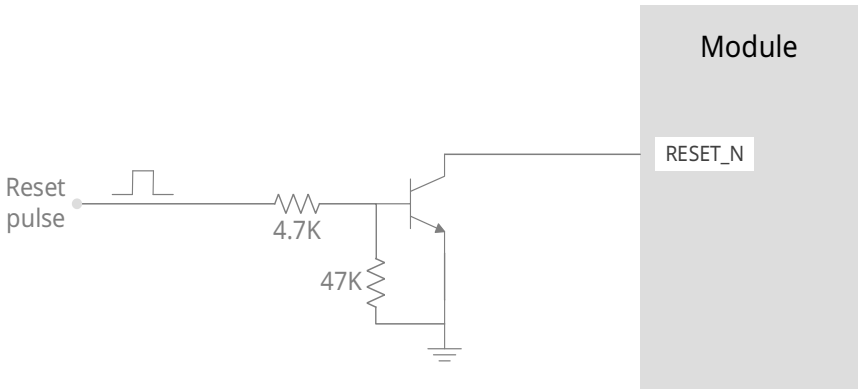



Figure 10. OC drive Reset circuit

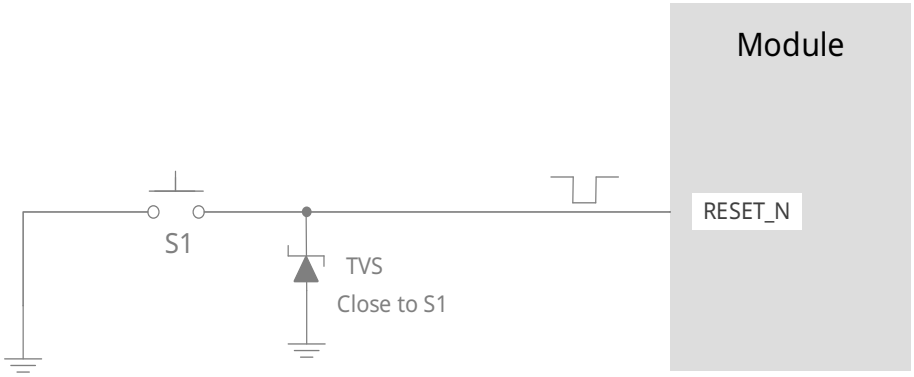



Figure 11. Reset push-botton circuit

- It is recommended to execute AT command to restart or operate PWRKEY to shutdown first, and use RESET_N only after a failed restart or shutdown.
- Ensure that PWRKEY and RESET_N do not have large load capacitance.

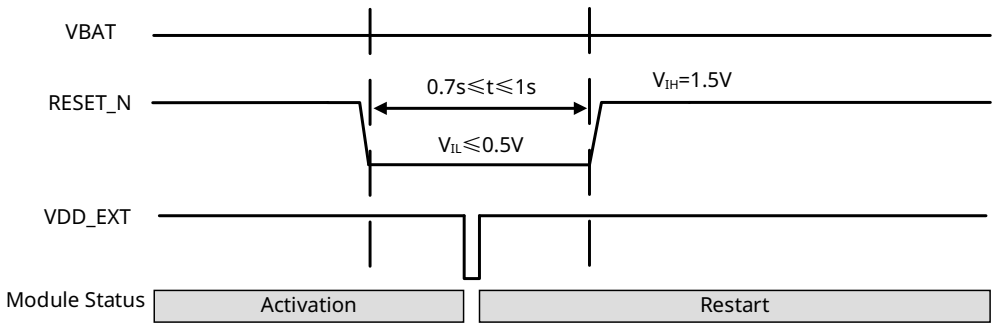



Figure 12. Reset timing sequence

# 4.4 PCIe Interface

The module supports one PCIe 2.0 interface and is backward compatible with the 1.0 interface. Support RC and EP* mode

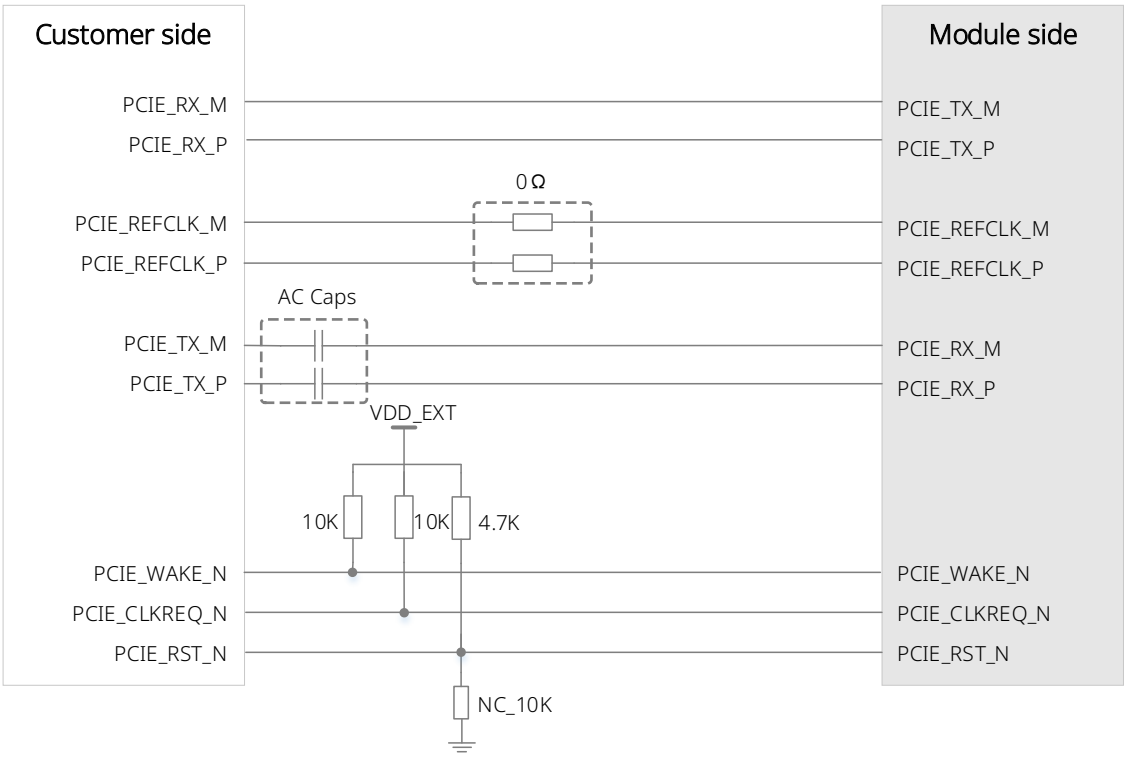



Figure 13. PCIe application circuit

PCIe 2.0 contains three sets of differential pairs: transmitting pair TX P/N, receiving pair RX P/N, and clock pair CLK P/N. The maximum transfer rate reaches 5Gbps. In PCB Layout, the following rules must be strictly followed:

- The differential signal pairs are required to be parallel wires with equal length, and the difference in length is less than 0.7mm.
- The trace length of differential signal pair shall be as short as possible, and the length of AP end should be controlled within 230mm.
- The impedance of differential signal pair traces is recommended to be 85Ω.
- Avoid discontinuous reference ground, such as segment and space.
- When routing differential signals across layers, the ground signal vias should be placed close to the signal vias. Each signal pair should have at least 1 to 3 ground signal vias, and the routing should not cross plane splits.
- Try to avoid bended traces and avoid introducing common-mode noise in the system, otherwise will influence the signal integrity and EMI of difference pairs. As shown in the following figure, the bending angle of all traces should be equal to or greater than 135°, the spacing between differential pair traces should be larger than 20mils, and the traces caused by bending should be greater than 1.5 times the width at least. When a serpentine trace is used for length match with another trace, the bended length of each segment should be at least 3 times the trace width (≥ 3W). The largest spacing between the

bended part of the serpentine trace and another differential trace must be less than 2 times the spacing of normal differential traces (S1 < 2S).

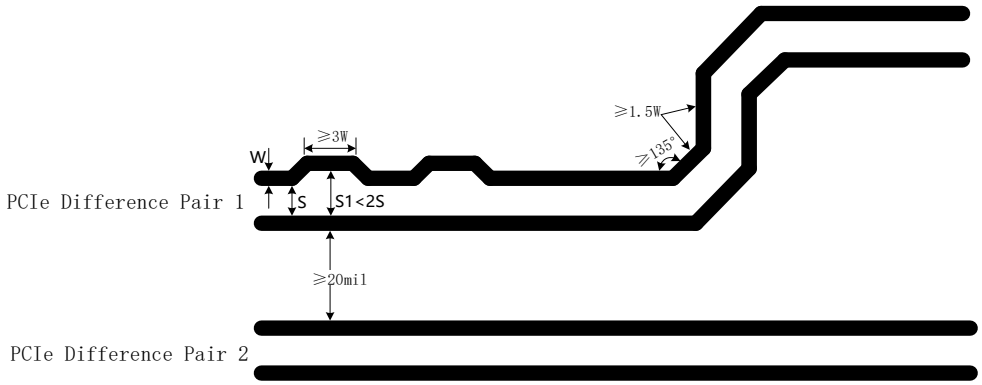



Figure 14. PCIe routing requirements

- The serpentine trace should be positioned near the unmatched end of the differential line, as shown in the following figure. However, there is no specific requirements for the length match of transmitting pair and receiving pair. That is, the length match is only required in the internal differential lines rather than between different differential pairs. The length match should be close to the signal pin and achieve length match through the small-angle bending design.

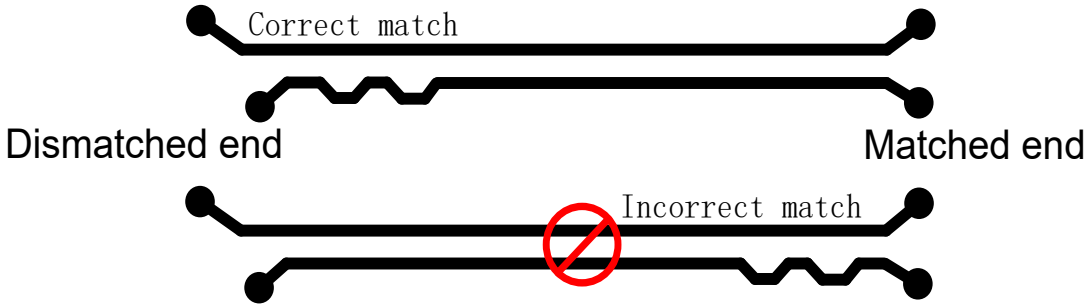



Figure 15. Length match design of differential pairs

## 4.5 USB Interfaces

The module provides a USB interface, conforms to the USB 2.0 specification, supports high-speed mode, up to 480Mbps, and is backward compatible with 12Mbps full-speed mode. USB interface supports master* and slave mode, which can be used for AT command communication, data transmission, software debugging, firmware upgrade, etc.

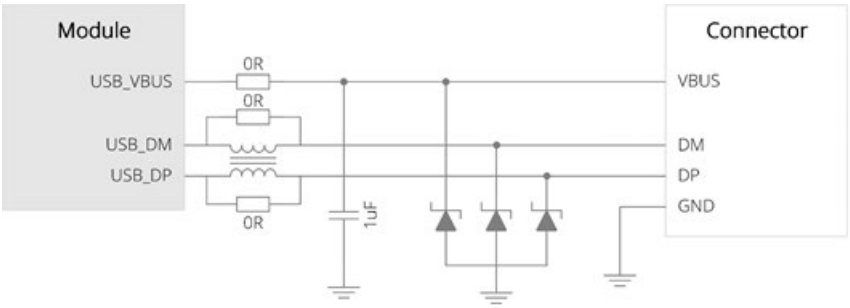



Figure 16. USB 2.0 reference design

It is recommended to connect a common-mode inductor in series between host and module to suppress EMI, and reserve 0R series resistance without patch by default. In order to meet the signal integrity requirements of USB data lines, the common mode inductor should be placed close to the module, resistors should be placed close to each other, and traces connecting test points should be kept as short as possible.

The USB 2.0 of the module includes both USB High-Speed (480Mbps) and USB Full-Speed (12Mbps) modes. The equivalent capacitance of the TVS diode on the differential signal lines should be less than 2pF. If there is no ESD risk for the USB interface, the TVS diode can be omitted.

Here are the layout design rules for USB 2.0:

- The differential impedance of USB_D- and USB_D+ signal lines should be controlled within 90Ω±10Ω.
- The length difference between the USB_D- and USB_D+ signal lines should be less than 2 mm, and they should be run in parallel. Avoid routing at right angles.
- It is recommended to route the USB_D- and USB_D+ signal lines on inner layers, with ground planes surrounding on the top, bottom, left and right sides of them for protection.

When not using the USB interface, it is recommended to use the USB 2.0 interface for firmware upgrades and reserve test points for debugging.

# 4.6 USIM Interfaces

The module has built-in USIM1 and USIM2 card interfaces, conforms to ETSI and IMT-2000 specifications, supports 1.8V or 3.0V (U)SIM cards, and supports dual card single standby function. The module identifies USIM1 by default and can be switched to USIM2 by the following AT command:

AT+GTDUALSIM=1, for more information please refer to *Fibocom_FG132_AT_Commands_User_Manual*

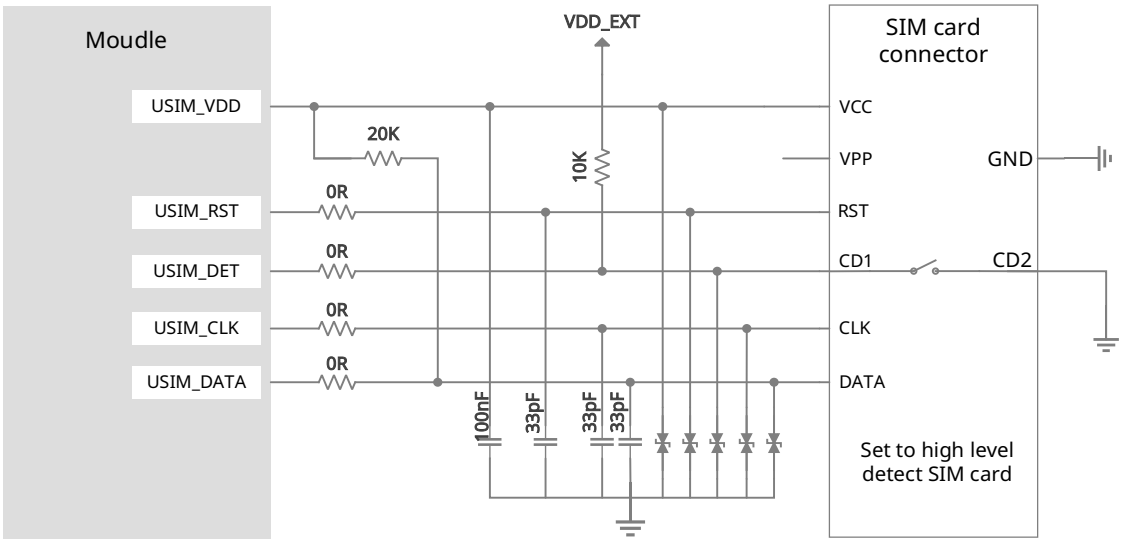



Figure 17. 8 pin SIM card reference circuit

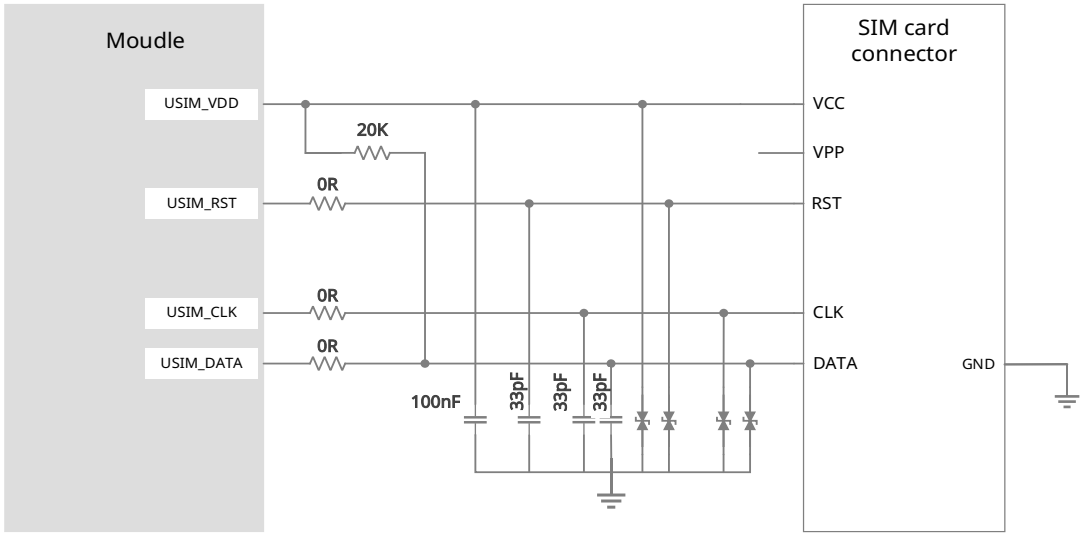



Figure 18. 6 pin SIM card reference circuit

The ESDBL5V0A1 model is recommended for TVS tubes in the above two SIM card reference designs. To ensure the stable operation of USIM cards, the following rules should be strictly followed in the design:

- Place the (U)SIM card slot close to the module and try to ensure that the length of the (U)SIM card signal trace does not exceed 200 mm.
- It is recommended to route (U)SIM card signal lines in the inner layer with a three-dimensional ground wrapped. It need to be kept away from power lines, crystals, magnetic devices, sensitive signals such as RF signals, analog signals, and noise signals generated by clocks and DC-DCs.
- To prevent crosstalk between the USIM_CLK signal and the USIM_DATA signal, the two traces should not be too close to each other, and a ground shield should be added between the two traces.
- (U)SIM card peripherals is placed as close as possible to the (U)SIM card slot. Add ESD protection

devices near the card slot, and the parasitic capacitance of the selected TVS tube is not greater than 15pF. At the same time, a 0Ω resistor is connected in series between the module and the (U)SIM card slot for debugging. A 33pF capacitor is connected in parallel to the USIM_DATA, USIM_CLK, and USIM_RST signal lines to filter out RF interference.

- For USIM_DATA, add a 20kΩ pull-up resistor close to the card slot to improve the anti-interference capability of the (U)SIM card.

The module implements hot plug function for the USIM card through the USIM_DET pin. A default high level represents that the SIM card is inserted, while a low level represents that the SIM card is removed. If the user does not need the hot plug function, float USIM_DET. In addition, the hot plug function of USIM card can be enabled and disabled by AT command.

Table 13. Hot plug function of USIM card

| AT Command | Function Description | Note |
|---|---|---|
| AT+MSMPD=1 | Enable the hot plug function detection of USIM card. | - - |
| AT+MSMPD=0 | Disable the USIM card hot plug detection function. | - - |

SIM1 hot plug is enabled and SIM2 hot plug is disabled by default. The AT+MSMPD/AT+SIMSWAPCFG command takes effect based on the GTDUALSIM parameter, for example: AT+GTDUALSIM=0, MSMPD and SIMSWAPCFG set hot plug and high/low level detection for SIM1, AT+GTDUALSIM=1, MSMPD and SIMSWAPCFG set hot plug and high/low level detection for SIM2.

## 4.7 UART Interfaces

The module supports three UART interfaces: main UART data transmission interface, debugging interface and coex interface. The interface functions are described as follows:

- UART1 data transmission interface supports 300bps, 600bps, 1200bps, 2400bps, 4800bps, 9600bps, 19200bps, 38400bps, 57600bps, 115200bps (default), 230400bps, 460800bps, 921600bps, 1Mbps, 2Mbps, 3Mbps and 4Mbps baud rates, mainly used to transmit data and send AT command.
- The DEG debugging interface supports 115200bps baud rate, used to transfer logs and enter the Linux console.
- Coexistence UART is only used for 5G/LTE & WLAN coexistence applications, not for other scenarios

The UART interface of the module operates at 1.8V voltage level. If the customer's host system operates at 3.3V or other voltage levels, an additional level shifting circuit is required.

The following figure shows the reference circuit of level shifting chip.

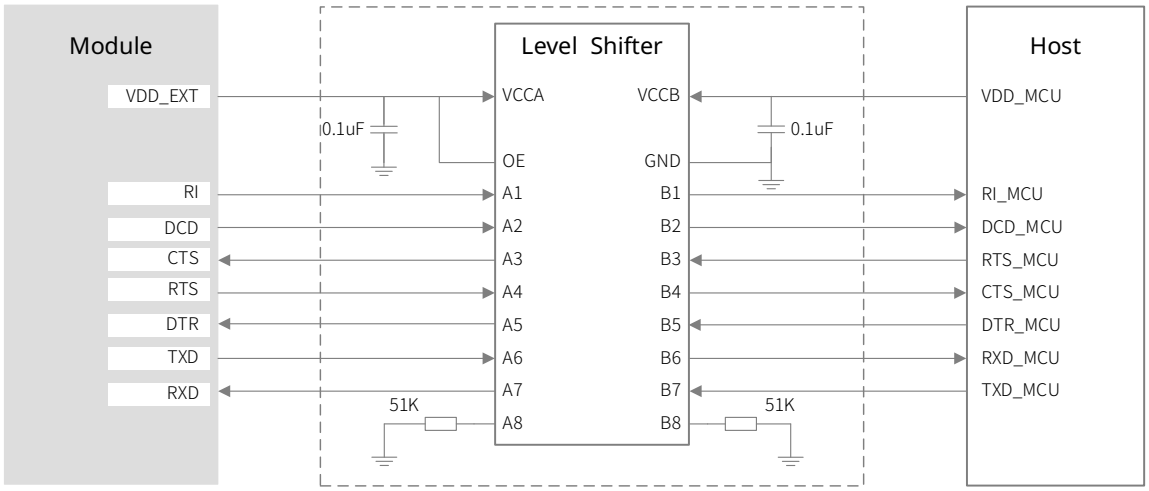



Figure 19. Reference circuit of level shifting chip

The following figure shows the transistor level shifting circuit, which is only suitable for applications with a baud rate not exceeding 460Kbps.

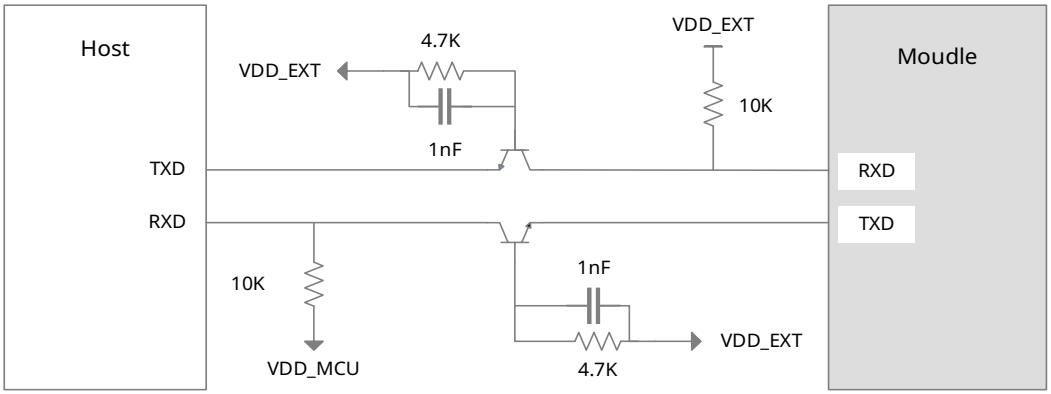



Figure 20. Transistor level shifting circuit

- It is recommended to reserve test points for Debug UART to facilitate debugging and capturing logs.
- UART baud rate adaptation, based on 115200, can adapt to 19200, 38400, 57600, and 115200 baud rates in at commands.

# 4.8 SPI Interfaces *

The SPI function of the module works in master mode, with a maximum clock speed of 50MHz. The reference circuit of SPI interface circuit is shown in the following figure.


Figure 21. SPI interface reference circuit

# 4.9 PCM and I2C Interfaces

The module provides a PCM interface and an I2C interface. The PCM interface supports the following two modes:

- Short Frame Mode: The module can be slave* or master device.
- Long frame mode: The module can only be a master device.

The module supports 16-bit linear encoding formats. The following timing diagrams are for short frame mode (PCM_SYNC=8kHz, PCM_CLK=2048kHz) and long frame mode (PCM_SYNC=8kHz, PCM_CLK=256kHz).

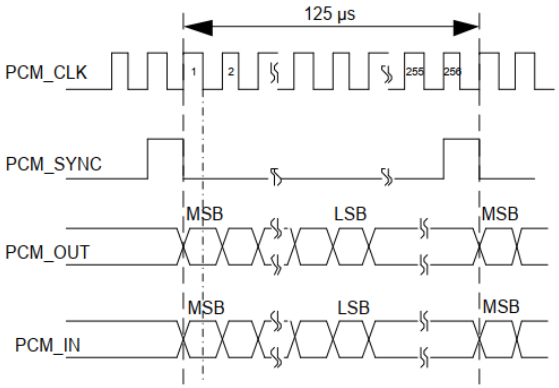



Figure 22. Timing diagram for short frame mode

In short frame mode, data is sampled on the falling edge of PCM_CLK and sent on the rising edge. The falling edge of PCM_SYNC represents a high valid bit. When PCM_SYNC reaches 8kHz, PCM_CLK supports 256kHz, 512kHz, 1024kHz and 2048kHz; when PCM_SYNC reaches 16kHz, PCM_CLK supports 4096kHz.

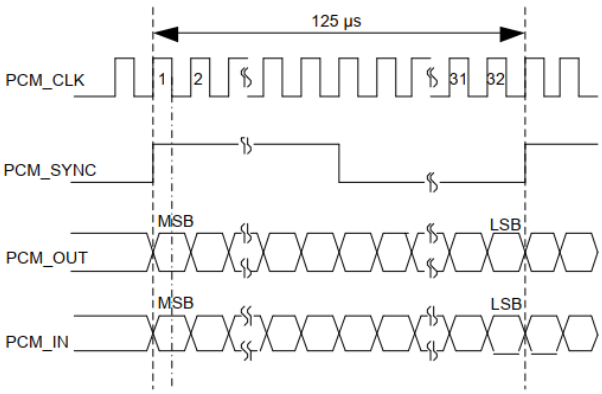



Figure 23. Timing diagram for short frame mode

In long frame mode, data is also sampled on the falling edge of PCM_CLK and sent on the rising edge. The rising edge of PCM_SYNC represents the high valid bit. When PCM_SYNC reaches 8kHz and the duty cycle is 50%, PCM_CLK supports 256kHz, 512kHz, 1024kHz, and 2048kHz.

The I2C_SDA and I2C_SCL interfaces require a VDD_EXT pull-up. The PCM external codec reference circuit is shown in the following figure:

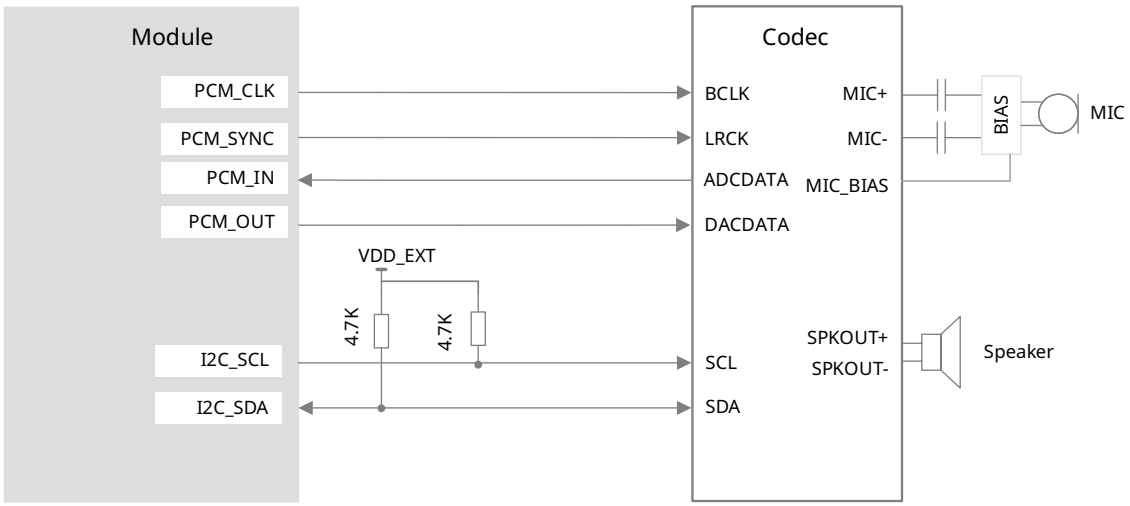



Figure 24. PCM external codec reference circuit

- It is recommended that RC (R=22Ω, C=22pF) circuits be reserved on the signal lines of the PCM (especially PCM_CLK).
- The module can only be used as a master device in both PCM interface applications and I2C interface applications.

# 4.10 Network Status Indicator Interfaces

The module provides three network status indication signal interfaces, NET_MODE and NET_STATUS are used to indicate the network registration status and network operation status of the module respectively,

and drive the corresponding LEDs at the same time.

Table 14. Network status

| Pin Name | Pin Level Status | Network Status |
|---|---|---|
| NET_MODE | High level | Registered to 5G network |
| | Low level | Others |
| NET_STATUS | Slow flash (200ms high/1800ms low) | Network search mode |
| | Slow flash (1800ms high/200ms low) | Standby status |
| | Quick flash (125ms high/125ms low) | Data transmission mode |
| | High level | Voice call |

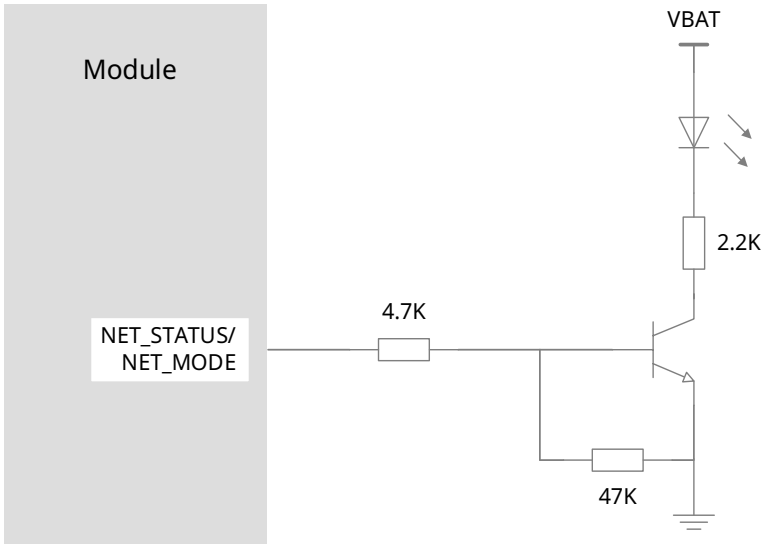



Figure 25. Network status indication reference circuit

STATUS is internally an open-drain current source used to indicate the operating status of the module. STATUS is low when the module is powered on normally. Otherwise, STATUS assumes a high impedance state.

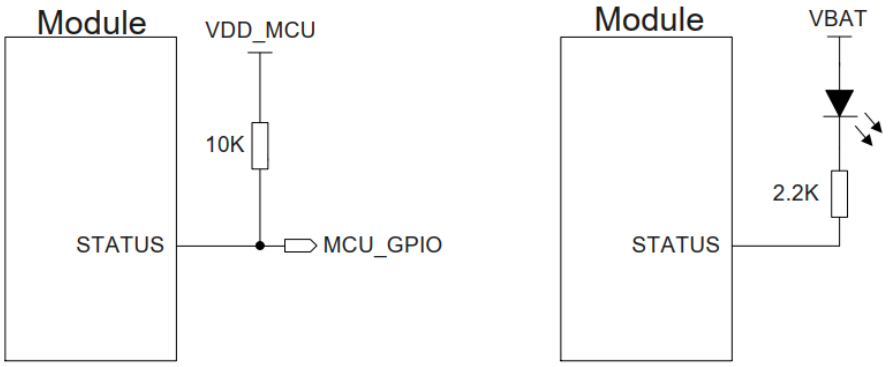



Figure 26. STATUS reference circuit

When VBAT is powered off, the status indication pin cannot indicate the module power-off status.

# 4.11 Flight Mode Control Interface

There are two flight mode control modes for the module:

- AT command control mode:

Default control mode. Send AT+CFUN=4 to enter flight mode and send AT+CFUN=1 to enter operating mode.

- Hardware control mode:

This function is disabled by default, and can be enabled by sending AT+GTFMODE=1 through USB. W_DISABLE# has a default internal pull-up inside the module. When W_DISABLE# is pulled up, the module enters the operating mode. When W_DISABLE# is pulled down, the module enters the flight mode. Sending AT+GTFMODE=0 can disable this function.

# 4.12 Sleep/Wake-up Interfaces

When the module is in the sleep state, the host can wake up the module by pulling the WAKEUP_IN or DTR pin down.

When the module is in sleep mode and there is an incoming call or message, the RI pin of the module will be automatically pulled down to wake up the host.

The wake-up mode and wake-up active level of the module can be configured through AT commands. For detailed description, refer to the sleep/wakeup function description document of relevant products.

# 4.13 USB_BOOT Interfaces

USB_BOOT is an emergency download pin. Pull up the pin and then power on the module, and the module automatically enters the download mode. The firmware of the module can be upgraded through USB interface. USB_BOOT is sensitive, so it is recommended to route it on the inner layer of the PCB and avoid sensitive signals such as power. Keep the trace length as short as possible to avoid low-frequency

interference.

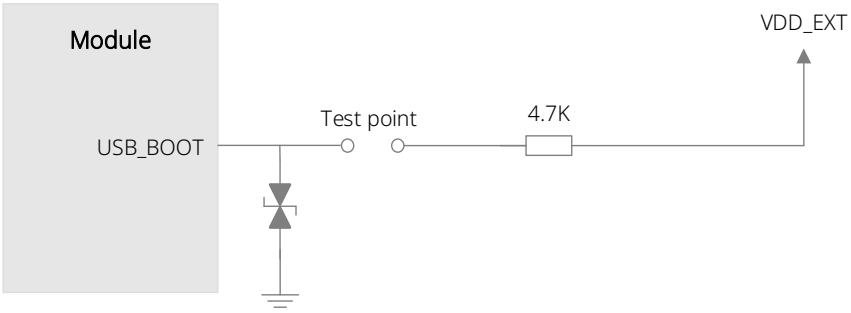



Figure 27. USB_BOOT circuit

Do not pull up to high level until the module is successfully powered on. It is recommended to reserve test points for VDD_EXT.

# 4.14 ADC Interfaces

The module provides two ADCs. The voltage value of ADC interface can be read by using the AT+MMAD command, and the measurement accuracy is 0.2mV. ADC traces need to be wrapped with ground, which can improve the accuracy of ADC voltage measurement.

Table 15. ADC electrical characteristics

| Pin Name | Input Voltage Min(V) | Input Voltage Max(V) |
|---|---|---|
| ADC0 | 0 | VBAT_BB |
| ADC1 | 0 | VBAT_BB |

- When VBAT_BB do not have power supply, the ADC interface should not connect to any input power supply
- Use a voltage divider resistor design for the ADC interface, otherwise it will reduce the measurement accuracy of the ADC

# 4.15 SGMII Interfaces

The module provides one SGMII interface with embedded Ethernet MAC and one MDIO management interface. The key features of the SGMII interface are as follows:

- Compliant with IEEE 802.3 standard
- Half/full duplex rates of 10Mbps, 100Mbps and 1000Mbps
- Compliant with IEEE 1588 standard and PTP protocol

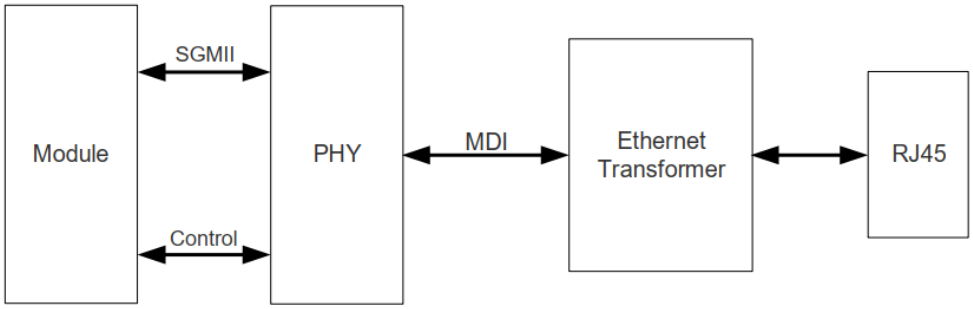



Figure 28. Ethernet application block diagram

To ensure good performance and reliability, refer to the following principles for SGMII signal design:

- SGMII interface data signals and control signals need to be away from power lines, crystal, magnetic devices, sensitive signals such as RF signals, analog signals, and noise signals generated by clocks, DC-DC, etc.
- The maximum length of SGMII interface differential data signal trace does not exceed 10 inches, and the length difference of RX and TX differential lines does not exceed 0.7 mm.
- The impedance of the differential data signal of the SGMII interface needs to be controlled within 90Ω ± 10%, and the reference ground plane is complete.
- Ensure that the trace distance between SGMII_RX and SGMII_TX and the distance between other adjacent signal lines is at least 3 times the line width.

# 5 Antenna Interfaces

## 5.1 Antenna Interfaces

Please read the antenna interface definition carefully and select the correct antenna interface for connection. For assistance, please contact the Fibocom technical personnel.

Table 16. Definition of antenna interfaces

| Pin Name | Function Description | TX | RX | Frequency range |
|---|---|---|---|---|
| ANT_MAIN | TRX | LTE: B1/2/3/4/5/7/8/12/13/14/17/18/19/20/25/26/28/30/B34/38/39/40/41/42/43/48/66/71<br>NR: n1/2/3/5/7/8/12/13/14/18/20/25/26/28/30/38/40/41/48/66/70/71/77/78/79 | LTE: B1/2/3/4/5/7/8/12/13/14/17/18/19/20/25/26/28/30/B34/38/39/40/41/42/43/48/66/71<br>NR: n1/2/3/5/7/8/12/13/14/18/20/25/26/28/30/38/40/41/48/66/70/71/77/78/79 | 617MHz~5GHz |
| ANT_DIV | DRX | - - | LTE: B1/2/3/4/5/7/8/12/13/14/17/18/19/20/25/26/28/30/B34/38/39/40/41/42/43/48/66/71<br>NR: n1/2/3/5/7/8/12/13/14/18/20/25/26/28/30/38/40/41/48/66/70/71/77/78/79 | 617MHz~5GHz |
| ANT_GNSS | GNSS | - - | GPS/GLONASS/BDS/Galileo/QZSS | 1166MHz~1606MHz |

## 5.2 Operating Frequency

Tables 17. Cellular frequency

| Operating Band | Standard | Tx (MHz) | Rx (MHz) |
|---|---|---|---|
| 5G NR | n1 | 1920~1980 | 2110~2170 |
| | n2 | 1850~1910 | 1930~1990 |
| | n3 | 1710~1785 | 1805~1880 |
| | n5 | 824~849 | 869~894 |
| | n7 | 2500~2570 | 2620~2690 |
| | n8 | 880~915 | 925~960 |

| Operating Band | Standard | Tx (MHz) | Rx (MHz) |
|---|---|---|---|
| | n12 | 699~716 | 729~746 |
| | n13 | 777~787 | 746~756 |
| | n14 | 788~798 | 758~768 |
| | n18 | 815~830 | 860~875 |
| | n20 | 832~862 | 791~821 |
| | n25 | 1850~1915 | 1930~1995 |
| | n26 | 814~849 | 859~894 |
| | n28 | 703~748 | 758~803 |
| | n30 | 2305~2315 | 2350~2360 |
| | n66 | 1710~1780 | 2110~2180 |
| | n70 | 1695~1710 | 1995~2010 |
| | n71 | 663~698 | 617~652 |
| | n38 | 2570~2620 | 2570~2620 |
| | n40 | 2300~2400 | 2300~2400 |
| | n41 | 2496~2690 | 2496~2690 |
| | n48 | 3550~3700 | 3550~3700 |
| | n77 | 3300~4200 | 3300~4200 |
| | n78 | 3300~3800 | 3300~3800 |
| | n79 | 4400~5000 | 4400~5000 |
| LTE FDD | Band 1 | 1920~1980 | 2110~2170 |
| | Band 2 | 1850~1910 | 1930~1990 |
| | Band 3 | 1710~1785 | 1805~1880 |
| | Band 4 | 1710~1755 | 2110~2155 |
| | Band 5 | 824~849 | 869~894 |
| | Band 7 | 2500~2570 | 2620~2690 |
| | Band 8 | 880~915 | 925~960 |
| | Band 12 | 699~716 | 729~746 |
| | Band 13 | 777~787 | 746~756 |
| | Band 14 | 788~798 | 758~768 |

| Operating Band | Standard | Tx (MHz) | Rx (MHz) |
|---|---|---|---|
| | Band 17 | 704~716 | 734~746 |
| | Band 18 | 815~830 | 860~875 |
| | Band 19 | 830~845 | 875~890 |
| | Band 20 | 832~862 | 791~821 |
| | Band 25 | 1850~1915 | 1930~1995 |
| | Band 26 | 814~849 | 859~894 |
| | Band 28 | 703~748 | 758~803 |
| | Band 30 | 2305~2315 | 2350~2360 |
| | Band 66 | 1710~1780 | 2110~2180 |
| | Band 71 | 663~698 | 617~652 |
| LTE TDD | Band 34 | 2010~2025 | 2010~2025 |
| | Band 38 | 2570~2620 | 2570~2620 |
| | Band 39 | 1880~1920 | 1880~1920 |
| | Band 40 | 2300~2400 | 2300~2400 |
| | Band 41 | 2496~2690 | 2496~2690 |
| | Band 42 | 3400~3600 | 3400~3600 |
| | Band 43 | 3600~3800 | 3600~3800 |
| | Band 48 | 3550~3700 | 3550~3700 |

## 5.3 Antenna Design Circuit

The following figure shows an antenna circuit for a cellular network:

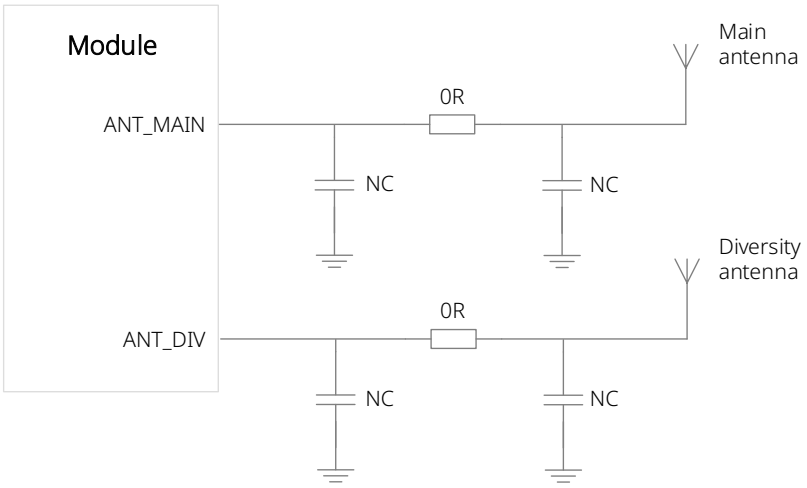



Figure 29. Cellular network antenna reference circuit

The following figure shows the GNSS active antenna. If the active antenna is not required, the dotted line part can be deleted. The circuit diagram of GNSS antenna is as follows:

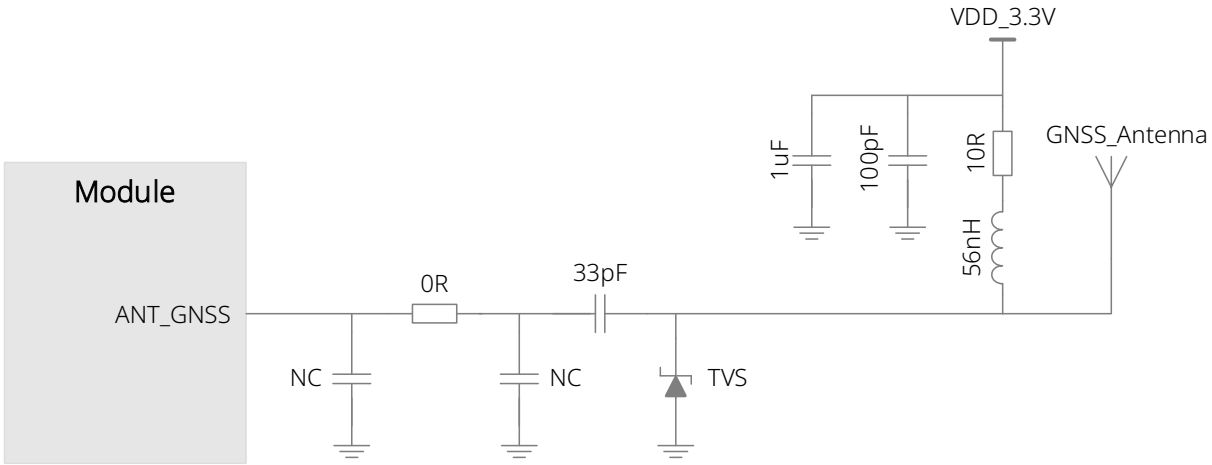



Figure 30. GNSS antenna reference circuit

- The TVS on GNSS antenna is recommended ESDSU5V0A1.
- If no active antenna is used, do not patch 1uF+100pF+10R+56nH power supply device, and retain other devices.

# 5.4 Antenna Performance Requirements

Input impedance: 50Ω

Input power: > 28dBm

VSWR: < 2:1

Antenna gain: < 3.6dBi

Antenna isolation: > 25dB

Insertion loss of antenna cable: LB (< 1GHz) < 0.3dB, MB (1GHz to 2.7GHz) < 0.8dB, HB (> 2.7GHz) < 1.2dB

## 5.5 PCB Layout Reference Design

In practical applications, the shorter the RF microstrip trace, the better. Impedance is usually closely related to the width (W) and thickness of the trace, the height (H) of the reference layer, the spacing (S) between the trace and the left and right sides of the ground, and the dielectric constant of the material. The impedance control model of RF microstrip line is divided into planar reference model and coplanar impedance model. Generally, if the planar reference model can meet the requirements, the coplanar impedance model should not be used.

- Planar reference model

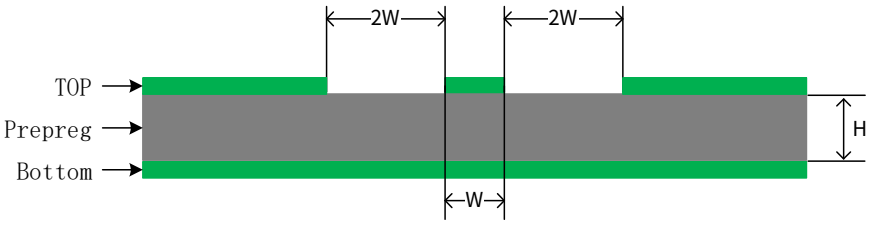



Figure 31. Planar reference model for a two-layer board

- Coplanar impedance model

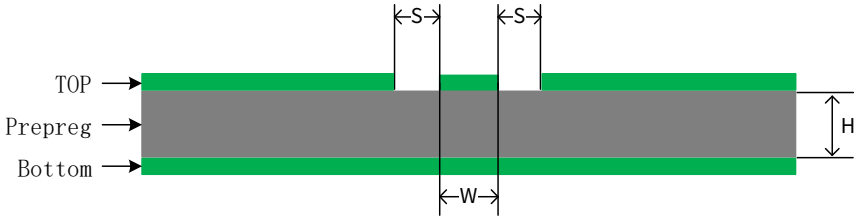



Figure 32. Coplanar impedance model for a two-layer board

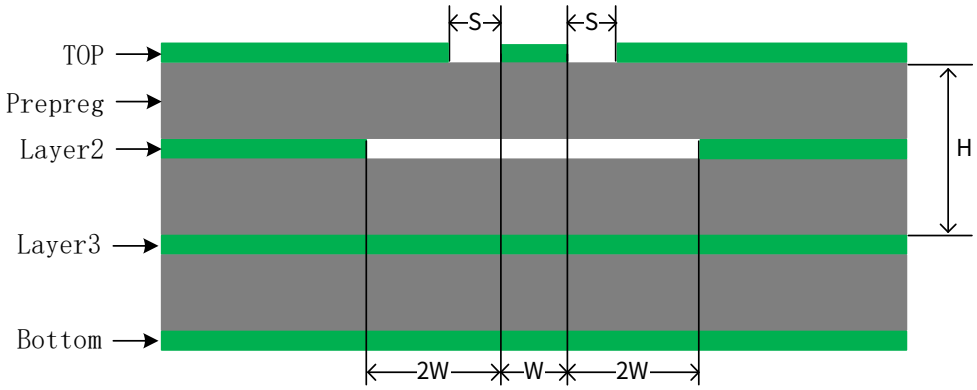



Figure 33. Coplanar impedance model for a four-layer board

The design rules are as follows:

- The RF trace impedance is controlled to 50Ω, and the reference ground must be kept intact.
- The RF routing should be curved as far as possible, and both sides of the routing should be protected by vias. The distance between vias and traces should be greater than 2 times the line width.
- There should be clearance below the RF connector, and the RF routing should be far away from the interference source to avoid crossing and paralleling with the interference source.

# 6 Electrical Characteristics

## 6.1 Logic Level

Table 18. IO logic level

| Description | Level | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| 1.8V IO input | High level | 1.26 | 1.8 | 2.1 | V |
| | Low level | -0.3 | 0 | 0.54 | V |
| 1.8V IO output | High level | 1.35 | 1.8 | 1.8 | V |
| | Low level | 0 | 0 | 0.45 | V |

## 6.2 Power consumption

The power consumption measurement is closely related to the working status of the module. The test conditions are as follows: the ambient temperature is 25 ° C, the power supply voltage is 3.8V, and the USB mode of the module is Device by default

Table 19. module power consumption

| Parameter | Mode | Condition | Current (mA) |
|---|---|---|---|
| $I_{off}$ | FG132-CN Power off | Power supply<br>Module power-off | 0.033 |
| | Other type Power off | Power supply<br>Module power-off | 0.028 |
| $I_{sleep}$ | Radio off | AT+CFUN=0<br>AT+GTLPMMODE=1 | 1.2 |
| | NR FDD | Paging cycle #64 frames (USB Disconnect) | 2.2 |
| | | Paging cycle #64 frames (USB Suspend) | TBD |
| | | Paging cycle #128 frames (USB Disconnect) | 1.9 |
| | | Paging cycle #128 frames (USB Suspend) | TBD |
| | | Paging cycle #256 frames (USB Disconnect) | 1.8 |
| | | Paging cycle #256 frames (USB Suspend) | TBD |
| | | EDRX=20.48s, PTW=1.28s, DRX=1.28s (USB Disconnect) | 1.6 |

| | | | |
|---|---|---|---|
| | | EDRX=20.48s, PTW=1.28s, DRX=1.28s (USB Suspend) | TBD |
| | | EDRX=40.96s, PTW=1.28s, DRX=1.28s (USB Disconnect) | 1.5 |
| | | EDRX=40.96s, PTW=1.28s, DRX=1.28s (USB Suspend) | TBD |
| | | EDRX=81.92s, PTW=1.28s, DRX=1.28s (USB Disconnect) | 1.4 |
| | | EDRX=81.92s, PTW=1.28s, DRX=1.28s (USB Suspend) | TBD |
| | | EDRX=81.92s, PTW=2.56s, DRX=1.28s (USB Disconnect) | 1.4 |
| | | EDRX=81.92s, PTW=2.56s, DRX=1.28s (USB Suspend) | TBD |
| | NR TDD | Paging cycle #64 frames (USB Disconnect) | 2.2 |
| | | Paging cycle #64 frames (USB Suspend) | TBD |
| | | Paging cycle #128 frames (USB Disconnect) | 2 |
| | | Paging cycle #128 frames (USB Suspend) | TBD |
| | | Paging cycle #256 frames (USB Disconnect) | 1.7 |
| | | Paging cycle #256 frames (USB Suspend) | TBD |
| | | EDRX=20.48s, PTW=1.28s, DRX=1.28s (USB Disconnect) | 1.6 |
| | | EDRX=20.48s, PTW=1.28s, DRX=1.28s (USB Suspend) | TBD |
| | | EDRX=40.96s, PTW=1.28s, DRX=1.28s (USB Disconnect) | 1.5 |
| | | EDRX=40.96s, PTW=1.28s, DRX=1.28s (USB Suspend) | TBD |
| | | EDRX=81.92s, PTW=1.28s, DRX=1.28s (USB Disconnect) | 1.4 |
| | | EDRX=81.92s, PTW=1.28s, DRX=1.28s (USB Suspend) | TBD |
| | | EDRX=81.92s, PTW=2.56s, DRX=1.28s (USB Disconnect) | 1.4 |
| | | EDRX=81.92s, PTW=2.56s, DRX=1.28s (USB Suspend) | TBD |
| | LTE FDD | Paging cycle #64 frames (USB Disconnect) | 2.3 |
| | | Paging cycle #64 frames (USB Suspend) | TBD |
| | | Paging cycle #128 frames (USB Disconnect) | 2.1 |
| | | Paging cycle #128 frames (USB Suspend) | TBD |
| | | Paging cycle #256 frames (USB Disconnect) | 1.9 |
| | | Paging cycle #256 frames (USB Suspend) | TBD |

| | | | |
|---|---|---|---|
| | | EDRX=20.48s, PTW=1.28s, DRX=1.28s (USB Disconnect) | 1.8 |
| | | EDRX=20.48s, PTW=1.28s, DRX=1.28s (USB Suspend) | TBD |
| | | EDRX=40.96s, PTW=1.28s, DRX=1.28s (USB Disconnect) | 1.7 |
| | | EDRX=40.96s, PTW=1.28s, DRX=1.28s (USB Suspend) | TBD |
| | | EDRX=81.92s, PTW=1.28s, DRX=1.28s (USB Disconnect) | 1.7 |
| | | EDRX=81.92s, PTW=1.28s, DRX=1.28s (USB Suspend) | TBD |
| | | EDRX=81.92s, PTW=2.56s, DRX=1.28s (USB Disconnect) | 1.7 |
| | | EDRX=81.92s, PTW=2.56s, DRX=1.28s (USB Suspend) | TBD |
| | LTE TDD | Paging cycle #64 frames (USB Disconnect) | 2.2 |
| | | Paging cycle #64 frames (USB Suspend) | TBD |
| | | Paging cycle #128 frames (USB Disconnect) | 2 |
| | | Paging cycle #128 frames (USB Suspend) | TBD |
| | | Paging cycle #256 frames (USB Disconnect) | 1.9 |
| | | Paging cycle #256 frames (USB Suspend) | TBD |
| | | EDRX=20.48s, PTW=1.28s, DRX=1.28s (USB Disconnect) | 1.8 |
| | | EDRX=20.48s, PTW=1.28s, DRX=1.28s (USB Suspend) | TBD |
| | | EDRX=40.96s, PTW=1.28s, DRX=1.28s (USB Disconnect) | 1.7 |
| | | EDRX=40.96s, PTW=1.28s, DRX=1.28s (USB Suspend) | TBD |
| | | EDRX=81.92s, PTW=1.28s, DRX=1.28s (USB Disconnect) | 1.7 |
| | | EDRX=81.92s, PTW=1.28s, DRX=1.28s (USB Suspend) | TBD |
| | | EDRX=81.92s, PTW=2.56s, DRX=1.28s (USB Disconnect) | 1.7 |
| | | EDRX=81.92s, PTW=2.56s, DRX=1.28s (USB Suspend) | TBD |
| $I_{IDLE}$ | NR FDD | Paging cycle #64 frames (USB Disconnect) | 10 |
| | | Paging cycle #64 frames (USB Connect) | 19 |
| | | EDRX=81.92, PTW=2.56s, DRX=1.28s (USB Disconnect) | 9 |
| | | EDRX=81.92, PTW=2.56s, DRX=1.28s (USB Connect) | 18 |
| | NR TDD | Paging cycle #64 frames (USB Disconnect) | 11 |

| | | | |
|---|---|---|---|
| | | Paging cycle #64 frames (USB Connect) | 19 |
| | | EDRX=81.92, PTW=2.56s, DRX=1.28s (USB Disconnect) | 9 |
| | | EDRX=81.92, PTW=2.56s, DRX=1.28s (USB Connect) | 18 |
| | LTE FDD | Paging cycle #64 frames (USB Disconnect) | 11 |
| | | Paging cycle #64 frames (USB Connect) | 20 |
| | | EDRX=81.92, PTW=2.56s, DRX=1.28s (USB Disconnect) | 10 |
| | | EDRX=81.92, PTW=2.56s, DRX=1.28s (USB Connect) | 19 |
| | LTE TDD | Paging cycle #64 frames (USB Disconnect) | 11 |
| | | Paging cycle #64 frames (USB Connect) | 20 |
| | | EDRX=81.92, PTW=2.56s, DRX=1.28s (USB Disconnect) | 10 |
| | | EDRX=81.92, PTW=2.56s, DRX=1.28s (USB Connect) | 19 |
| $I_{ACTIVE}$ | NR FDD | NR FDD Data transfer n1 @+23dBm | 610 |
| | | NR FDD Data transfer n2 @+23dBm | 610 |
| | | NR FDD Data transfer n3 @+23dBm | 720 |
| | | NR FDD Data transfer n5 @+23dBm | 600 |
| | | NR FDD Data transfer n7 @+23dBm | 750 |
| | | NR FDD Data transfer n8 @+23dBm | 560 |
| | | NR FDD Data transfer n12 @+23dBm | 600 |
| | | NR FDD Data transfer n13 @+23dBm | 600 |
| | | NR FDD Data transfer n14 @+23dBm | 560 |
| | | NR FDD Data transfer n18 @+23dBm | 600 |
| | | NR FDD Data transfer n20 @+23dBm | 650 |
| | | NR FDD Data transfer n25 @+23dBm | 650 |
| | | NR FDD Data transfer n26 @+23dBm | 610 |
| | | NR FDD Data transfer n28 @+23dBm | 610 |
| | | NR FDD Data transfer n30 @+23dBm | 780 |
| | | NR FDD Data transfer n66 @+23dBm | 650 |

| | | | |
|---|---|---|---|
| | | NR FDD Data transfer n70 @+23dBm | 650 |
| | | NR FDD Data transfer n71 @+23dBm | 580 |
| | NR TDD | NR TDD Data transfer n38 @+23dBm | 250 |
| | | NR TDD Data transfer n40 @+23dBm | 250 |
| | | NR TDD Data transfer n41 @+23dBm | 250 |
| | | NR TDD Data transfer n48 @+23dBm | 250 |
| | | NR TDD Data transfer n77 @+23dBm | 250 |
| | | NR TDD Data transfer n78 @+23dBm | 250 |
| | | NR TDD Data transfer n79 @+23dBm | 250 |
| | LTE FDD | LTE FDD Data transfer Band 1 @+23dBm | 650 |
| | | LTE FDD Data transfer Band 2 @+23dBm | 650 |
| | | LTE FDD Data transfer Band 3 @+23dBm | 720 |
| | | LTE FDD Data transfer Band 4 @+23dBm | 650 |
| | | LTE FDD Data transfer Band 5 @+23dBm | 650 |
| | | LTE FDD Data transfer Band 7 @+23dBm | 750 |
| | | LTE FDD Data transfer Band 8 @+23dBm | 600 |
| | | LTE FDD Data transfer Band 12 @+23dBm | 650 |
| | | LTE FDD Data transfer Band 13 @+23dBm | 650 |
| | | LTE FDD Data transfer Band 14 @+23dBm | 550 |
| | | LTE FDD Data transfer Band 17 @+23dBm | 650 |
| | | LTE FDD Data transfer Band 18 @+23dBm | 600 |
| | | LTE FDD Data transfer Band 19 @+23dBm | 600 |
| | | LTE FDD Data transfer Band 20 @+23dBm | 650 |
| | | LTE FDD Data transfer Band 25 @+23dBm | 650 |
| | | LTE FDD Data transfer Band 26 @+23dBm | 650 |
| | | LTE FDD Data transfer Band 28 @+23dBm | 600 |
| | | LTE FDD Data transfer Band 30 @+23dBm | 750 |

| | | | |
|---|---|---|---|
| | | LTE FDD Data transfer Band 66 @+23dBm | 650 |
| | | LTE FDD Data transfer Band 71 @+23dBm | 600 |
| | LTE TDD | LTE TDD Data transfer Band 34 @+23dBm | 350 |
| | | LTE TDD Data transfer Band 38 @+26dBm | 600 |
| | | LTE TDD Data transfer Band 39 @+23dBm | 300 |
| | | LTE TDD Data transfer Band 40 @+26dBm | 650 |
| | | LTE TDD Data transfer Band 41 @+26dBm | 600 |
| | | LTE TDD Data transfer Band 42 @+26dBm | 500 |
| | | LTE TDD Data transfer Band 43 @+26dBm | 450 |
| | | LTE TDD Data transfer Band 48 @+23dBm | 350 |

The above power consumption data is the average measured value, Due to different test condition and consistency, the data floating range is normal within 10%

## 6.3 Max Output Power

The maximum transmit power refers to the power at the antenna pin of the module at the ambient temperature of 25 degrees Celsius. Users should fully consider the insertion loss on the radio frequency channel when designing, so as to avoid excessive insertion loss affecting TRP indicators. The maximum transmit power of FG132 series modules is as follows:

Table 20. All Band TX Power

| Mode | Band | Tx Power（dBm） | Note |
|---|---|---|---|
| NR FDD | n1 | 23±2 | 10MHz Bandwidth，inner full |
| | n2 | 23±2 | 10MHz Bandwidth，inner full |
| | n3 | 23±2 | 10MHz Bandwidth，inner full |
| | n5 | 23±2 | 10MHz Bandwidth，inner full |
| | n7 | 23±2 | 10MHz Bandwidth，inner full |
| | n8 | 23±2 | 10MHz Bandwidth，inner full |
| | n12 | 23±2 | 10MHz Bandwidth，inner full |
| | n13 | 23±2 | 10MHz Bandwidth，inner full |

| Mode | Band | Tx Power（dBm） | Note |
|---|---|---|---|
| | n14 | 23±2 | 10MHz Bandwidth，inner full |
| | n18 | 23±2 | 10MHz Bandwidth，inner full |
| | n20 | 23±2 | 10MHz Bandwidth，inner full |
| | n25 | 23±2 | 10MHz Bandwidth，inner full |
| | n26 | 23±2 | 10MHz Bandwidth，inner full |
| | n28 | 23±2 | 10MHz Bandwidth，inner full |
| | n30 | 23±2 | 10MHz Bandwidth，inner full |
| | n66 | 23±2 | 10MHz Bandwidth，inner full |
| | n70 | 23±2 | 10MHz Bandwidth，inner full |
| | n71 | 23±2 | 10MHz Bandwidth，inner full |
| NR TDD | n38 | 23±2 | 20MHz Bandwidth，inner full |
| | n40 | 23±2 | 20MHz Bandwidth，inner full |
| | n41 | 23±2 | 20MHz Bandwidth，inner full |
| | n48 | 23±2 | 20MHz Bandwidth，inner full |
| | n77 | 23±2 | 20MHz Bandwidth，inner full |
| | n78 | 23±2 | 20MHz Bandwidth，inner full |
| | n79 | 23±2 | 20MHz Bandwidth，inner full |
| LTE FDD | Band 1 | 23±2 | 10MHz Bandwidth，1 RB |
| | Band 2 | 23±2 | 10MHz Bandwidth，1 RB |
| | Band 3 | 23±2 | 10MHz Bandwidth，1 RB |
| | Band 4 | 23±2 | 10MHz Bandwidth，1 RB |
| | Band 5 | 23±2 | 10MHz Bandwidth，1 RB |
| | Band 7 | 23±2 | 10MHz Bandwidth，1 RB |
| | Band 8 | 23±2 | 10MHz Bandwidth，1 RB |
| | Band 12 | 23±2 | 10MHz Bandwidth，1 RB |
| | Band 13 | 23±2 | 10MHz Bandwidth，1 RB |
| | Band 14 | 23±2 | 10MHz Bandwidth，1 RB |
| | Band 17 | 23±2 | 10MHz Bandwidth，1 RB |
| | Band 18 | 23±2 | 10MHz Bandwidth，1 RB |
| | Band 19 | 23±2 | 10MHz Bandwidth，1 RB |

| Mode | Band | Tx Power（dBm） | Note |
|---|---|---|---|
| | Band 20 | 23±2 | 10MHz Bandwidth，1 RB |
| | Band 25 | 23±2 | 10MHz Bandwidth，1 RB |
| | Band 26 | 23±2 | 10MHz Bandwidth，1 RB |
| | Band 28 | 23±2 | 10MHz Bandwidth，1 RB |
| | Band 30 | 23±2 | 10MHz Bandwidth，1 RB |
| | Band 66 | 23±2 | 10MHz Bandwidth，1 RB |
| | Band 70 | 23±2 | 10MHz Bandwidth，1 RB |
| | Band 71 | 23±2 | 10MHz Bandwidth，1 RB |
| LTE TDD | Band 34 | 23±2 | 10MHz Bandwidth，1 RB |
| | Band 38 | 26±2 | 10MHz Bandwidth，1 RB |
| | Band 39 | 23±2 | 10MHz Bandwidth，1 RB |
| | Band 40 | 26±2 | 10MHz Bandwidth，1 RB |
| | Band 41 | 26±2 | 10MHz Bandwidth，1 RB |
| | Band 42 | 26±2 | 10MHz Bandwidth，1 RB |
| | Band 43 | 26±2 | 10MHz Bandwidth，1 RB |
| | Band 48 | 23±2 | 10MHz Bandwidth，1 RB |

## 6.4 Receiving Sensitivity

Receiving sensitivity refers to the sensitivity at the antenna pin of the module at an ambient temperature of 25 degrees Celsius. Users should fully consider the insertion loss on the radio frequency channel when designing, so as to avoid excessive insertion loss affecting the TIS index.

Table 21. Dual-antenna receiving sensitivity (dBm)

| Band | PRX | DRX | PRX+DRX | 3GPP-Requirement |
|---|---|---|---|---|
| 5G NR n1 (20M) | -95.5 | -96 | -98.5 | -93.8 |
| 5G NR n2 (20M) | -96 | -96 | -99 | -91.8 |
| 5G NR n3 (20M) | -95.5 | -96 | -98.5 | -90.8 |
| 5G NR n5 (20M) | -96 | -97 | -99 | -90.8 |
| 5G NR n7 (20M) | -95 | -96 | -98 | -91.8 |
| 5G NR n8 (20M) | -95.5 | -96.5 | -98.5 | -85.5 |
| 5G NR n12 (10M) | -98 | -98 | -101 | -93.8 |
| 5G NR n13 (10M) | -98.5 | -98.5 | -101 | -93.8 |
| 5G NR n14 (10M) | -98.5 | -98.5 | -101 | -93.8 |

| Band | PRX | DRX | PRX+DRX | 3GPP-Requirement |
|---|---|---|---|---|
| 5G NR n18 (10M) | -98.5 | -100 | -102 | -93.8 |
| 5G NR n20 (20M) | -95.5 | -96.5 | -98.5 | -89.8 |
| 5G NR n25 (20M) | -96 | -96 | -99 | -90.3 |
| 5G NR n26 (20M) | -95.5 | -96.5 | -98.5 | -87.6 |
| 5G NR n28 (20M) | -96 | -96.5 | -99 | -90.8 |
| 5G NR n30 (10M) | -98 | -98 | -101 | -95.8 |
| 5G NR n38 (20M) | -96.5 | -95 | -99 | -93.8 |
| 5G NR n40 (20M) | -95 | -95.5 | -98.5 | -93.8 |
| 5G NR n41 (20M) | -96.5 | -95 | -98 | -91.8 |
| 5G NR n48 (20M) | -96.5 | -96 | -99.5 | -92.8 |
| 5G NR n66 (20M) | -96 | -96 | -99 | -93.3 |
| 5G NR n70 (15M) | -97.5 | -97.5 | -100 | -95 |
| 5G NR n71 (20M) | -96 | -95.5 | -98.5 | -86 |
| 5G NR n77 (20M) | -96.5 | -96 | -99.5 | -92.3 |
| 5G NR n78 (20M) | -96.5 | -96 | -99.5 | -92.8 |
| 5G NR n79 (20M) | -96 | -96 | -99 | -92.8 |
| LTE Band 1(10M) | -98.5 | -99 | -102 | -96.3 |
| LTE Band 2(10M) | -99 | -99 | -102 | -94.3 |
| LTE Band 3(10M) | -98.5 | -98.5 | -101.5 | -93.3 |
| LTE Band 4(10M) | -98.5 | -99 | -102 | -96.3 |
| LTE Band 5(10M) | -99 | -100 | -102.5 | -94.3 |
| LTE Band 7(10M) | -98 | -99 | -101.5 | -94.3 |
| LTE Band 8(10M) | -99 | -100 | -102.5 | -93.3 |
| LTE Band 12(10M) | -98.5 | -98.5 | -101.5 | -93.3 |
| LTE Band 13(10M) | -98.5 | -99 | -101.5 | -93.3 |
| LTE Band 14(10M) | -98.5 | -98.5 | -101.5 | -93. |
| LTE Band 17(10M) | -98.5 | -99 | -101.5 | -93.3 |
| LTE Band 18(10M) | -99 | -100 | -102.5 | -96.3 |
| LTE Band 19(10M) | -99 | -100 | -102.5 | -96.3 |
| LTE Band 20(10M) | -99 | -99.5 | -102 | -93.3 |
| LTE Band 25(10M) | -99 | -99 | -102 | -92.8 |

| Band | PRX | DRX | PRX+DRX | 3GPP-Requirement |
|---|---|---|---|---|
| LTE Band 26(10M) | -99 | -99.5 | -102.5 | -93.8 |
| LTE Band 28(10M) | -99.5 | -99.5 | -102 | -94.8 |
| LTE Band 30(10M) | -98 | -98 | -101.5 | -95.3 |
| LTE Band 34(10M) | -98.5 | -98.5 | -101.5 | -96.3 |
| LTE Band 38(10M) | -99 | -97.5 | -101.5 | -96.3 |
| LTE Band 39(10M) | -98.5 | -99 | -101.5 | -96.3 |
| LTE Band 40(10M) | -97 | -98 | -101 | -96.3 |
| LTE Band 41(10M) | -98.5 | -97.5 | -101 | -94.3 |
| LTE Band 42(10M) | -99 | -99 | -102 | -95 |
| LTE Band 43(10M) | -99 | -99 | -102 | -95 |
| LTE Band 48(10M) | -99 | -99 | -102 | -95 |
| LTE Band 66(10M) | -98.5 | -99 | -102 | -95.8 |
| LTE Band 71(10M) | -99.5 | -98.5 | -101.5 | -93.5 |

## 6.5 GNSS

The module supports multiple positioning systems including GPS/Beidou/GLONASS/Galileo. The module is embedded with LNA, which can effectively improve the sensitivity of GNSS. Test conditions: Power supply voltage 3.8V, ambient temperature 25°C.

Table 22. GNSS performance

| Parameter | Description (instrument test) | Typical Result | Unit |
|---|---|---|---|
| Sensitivity | Acquisition | -146 | dBm |
| | Tracking | -157 | dBm |
| C/N | -130dBm | 38.5 | dB-Hz |
| TTFF | Cold Start | 31 | S |
| | Warm Start | 28 | S |
| | Hot Start | 2 | S |
| Static accuracy | CEP (50% @-130dBm) | 1 | m |

Table 23. GNSS band

| Mode | Band | Unit |
|---|---|---|
| GPS/QZSS | L1: 1575.42 | MHz |
| | L5: 1176.45 | MHz |
| GLONASS | L1：1602 | MHz |

| Mode | Band | Unit |
|---|---|---|
| Beidou | B1I：1561.098 | MHz |
| | B1C：1575.42 | MHz |
| | B2A：1176.45 | MHz |
| Galileo | E1: 1575.42 | MHz |
| | E5a：1176.45 | MHz |

## 6.6 Electrostatic Protection

The module is a precise electronic product. If electrostatic protection measures are not taken, permanent damage may be caused to the module. In the process of R & D, debugging, production, assembly, testing and other links, ESD protection measures should be taken. The ESD protection level at 25℃ ambient temperature and 45% humidity is described in the following table.

Table 24. ESD protection level

| Location | Air Discharge | Contact Discharge |
|---|---|---|
| Antenna GND | ±15KV | ±8KV |
| Antenna interface | N/A | ±8KV |

- The data is tested based on the development board of Fibocom.
- ESD performance is strongly related to PCB design, and key control signals should be protected.
- When designing the whole machine, pay attention to maintaining the integrity and connectivity of GND.

## 6.7 Reliability

The reliability test of Fibocom is carried out at industrial level, and the test results of each item are as follows:

Table 25. Reliability test result

| Test Item | Test Condition |
|---|---|
| High temperature aging | 85℃, 168H/504H/1008H |
| High temperature and humidity | 85℃ , 85%RH, 168H/504H/1008H |
| Corner test | High and low temperature, high and low humidity, high and low voltage, six groups of combinations, and each combination runs for |

| Test Item | Test Condition |
|---|---|
| | 24 hours |
| Temperature shock | 90/-45°C, 200C |
| Random vibration | Frequency range: 200Hz to 2000Hz, PSD=0.04 g2/Hz, one hour for X/Y/Z axis |
| Monomer drop | 1m, 6 sides and 2 wheels |
| Mechanical collision | Peak acceleration: 180m/s2<br>Pulse duration: 6ms<br>Number of collisions: 1000 |
| Low temperature boot | -40°C, 30 minutes off/5 minutes idle, 3 days |
| Condensation test | 3 days (3 cycles):<br>• First and second cycles with cold cycle<br>• Third cycle without cold cycle |
| Temperature cycle | 85°C/-40°C; 10°C/min; 10min; 240 cycles |
| Sinusoidal vibration | Amplitude: 3.0G peak to peak<br>Frequency: 5Hz to 500Hz<br>Sweep frequency: 0.5 Octave/min, linear<br>Each axis: 2H |
| Salt spray | Neutral salt spray, 48H |

# 6.8 Thermal Design

## 6.8.1 Main Board

Main board design suggestions:

Increase PCB size, and keep the module away from other heat source devices.

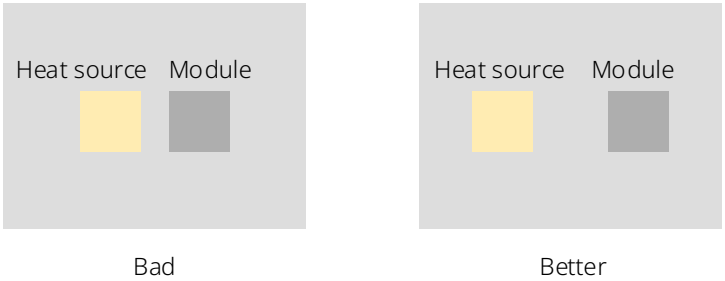



Figure 34. PCB layout

Increase PCB layers and the copper area at each layer.

Add adequate paths under and near the module. Plated holes boast better cooling effect than buried holes and blind holes. Vertically stacked paths boast better cooling effect than staggered paths.

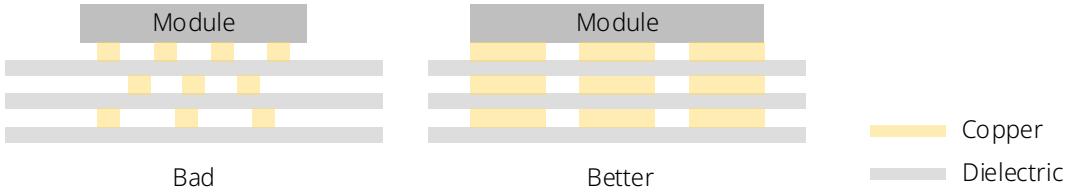



Figure 35. PCB stackup

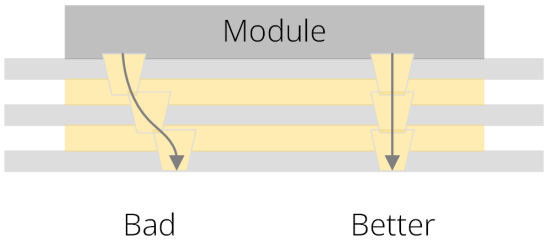



Figure 36. PCB drill hole

## 6.8.2 Product Structure

Recommendations for product structure:

Reduce the distance between module and heat sink and shell. Thermal conductive material thickness should not exceed 3 mm.

The thermal conduction path is shown in the following figure.

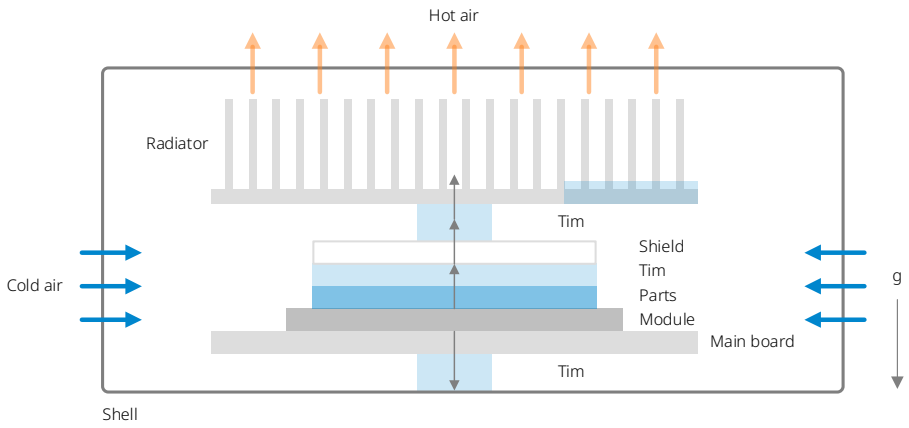



Figure 37. Heat conduction path

Use shell material with better thermal conductivity to facilitate cooling. Thermal conductivity sequence: Al > Fe > Plastic

Place the heat sink above the module.

Allow direct contact between the heat sink and thermal conductive material on the module if the heat sink can be exposed to the product surface.

Consider convection if the product has cooling holes.

# 7 Structure Specifications

## 7.1 Physical Appearance

Module physical appearance is shown in the following figures.


Figure 38. Top view 1


Figure 39. Top view 2


Figure 40. Top view 3


Figure 41. Top view 4

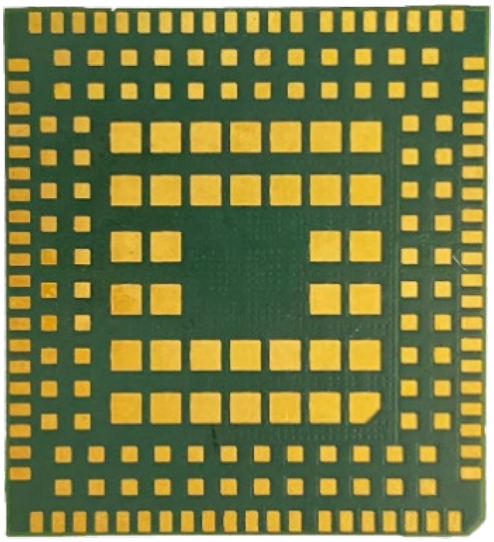


Figure 42. Bottom view

The pictures are for reference only. Please refer to the actual product for details.

## 7.2 Structure Dimensions

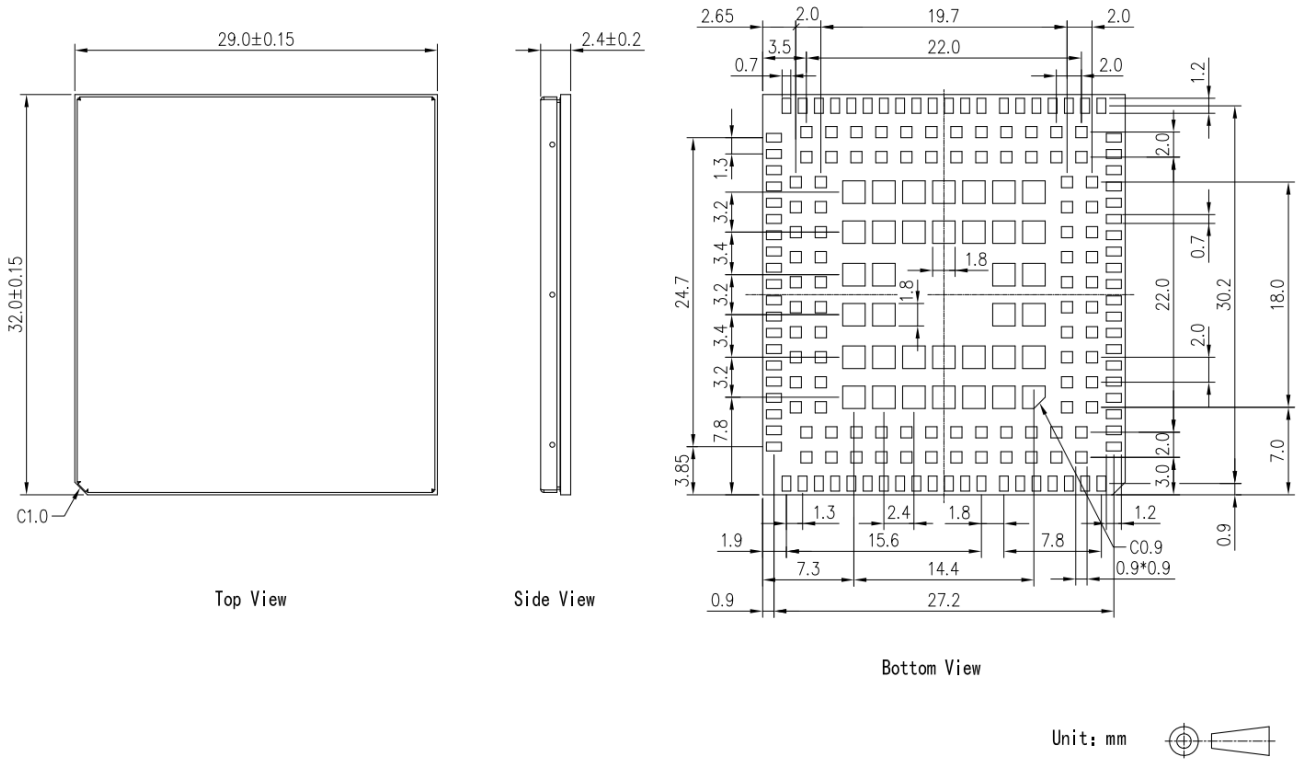



Figure 43. Structure dimensions

To ensure the SMT quality of the components and easy to maintain operations, the distance between the modules on the customer's PCB and other components should be at least 3mm.

## 7.3 PCB Package

When user design module PCB package, it recommend pattern that users refer to the *Fibocom_FG132_Package* file provided by our company

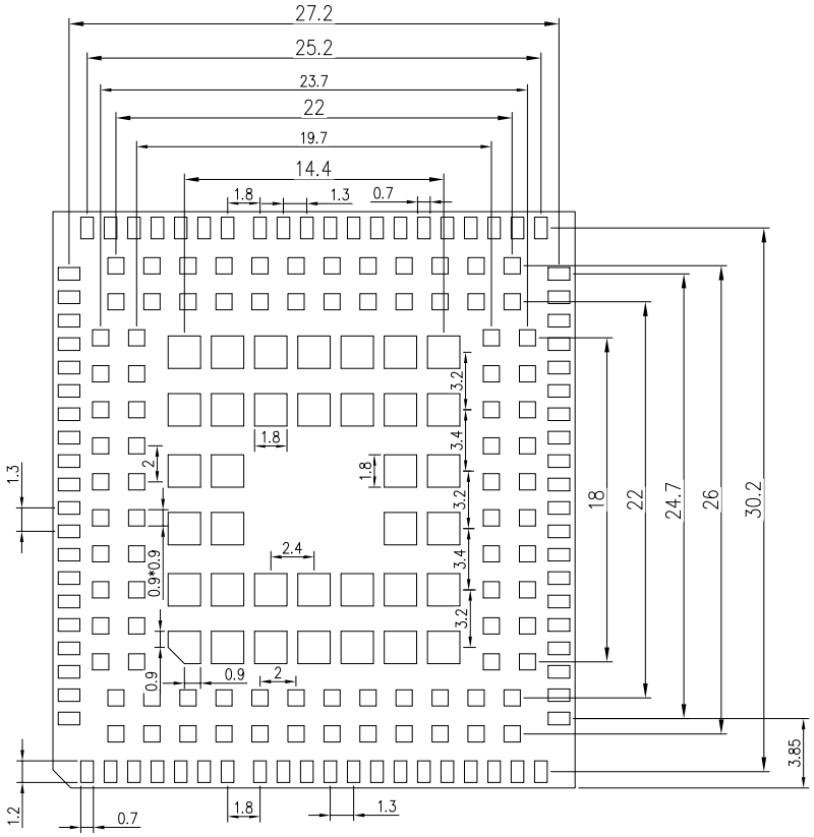



Figure 44. PCB package (unit: mm)

# 8 Storage, Production and Packaging

## 8.1 Storage Conditions

Storage Conditions:

Modules are shipped in vacuum sealed bags. The module has a humidity sensitivity level of 3 (MSL 3) and its storage is subject to the following conditions:

- Recommended storage conditions: The temperature is 23±5°C, and the relative humidity is 35% to 70%.
- Storage period of sealed vacuum packaging: 12 months.
- Under workshop conditions with a temperature of 23±5°C and relative humidity below 60%, the shelf life of the module after unpacking is 168 hours. Under these conditions, the module can be directly used for reflow production or other high temperature operations. Otherwise, the module needs to be stored in an environment with a relative humidity of less than 10% to keep the module dry.
- If the module is in the following conditions, pre-baking is required to prevent moisture-sensitive modules from experiencing PCB bubbling, cracking, and delamination during high-temperature soldering:
  - The storage temperature and humidity do not meet the recommended storage conditions.
  - The unpacked module does not meet the recommended conditions.
  - Vacuum packaging leakage, bulk materials.
  - Before module repair.

Baking treatment of modules:

- Baking at 120±5°C for 8 hours;
- The module of secondary baking must be soldered within 24 hours after baking, otherwise it still needs to be stored in the drying oven.

## 8.2 SMT Production

Module steel mesh design, solder paste and furnace temperature control please refer to *Fibocom FG132 SMT Application Design Notes*

## 8.3 Packaging Specifications

The module adopts tape packaging, so that the storage, transportation and the usage of the module can be protected to the greatest extent. Please read the packing instructions carefully to avoid damaging the product.

The product package is divided into three layers:

- Outer packaging: Hard card box
- Vacuum packaging: Anti-static sealed vacuum bag
- Inner packaging: Tape packaging

The module is a precise electronic product, and may be permanently damaged if you do not take correct ESD measures.

The module is moisture sensitive, please avoid moistening the product to prevent permanent damage.

Each roll is packed with 200 pcs, each box is packed with 1 rolls, and each hard carton box is packed with 4 boxes.

### Packaging process

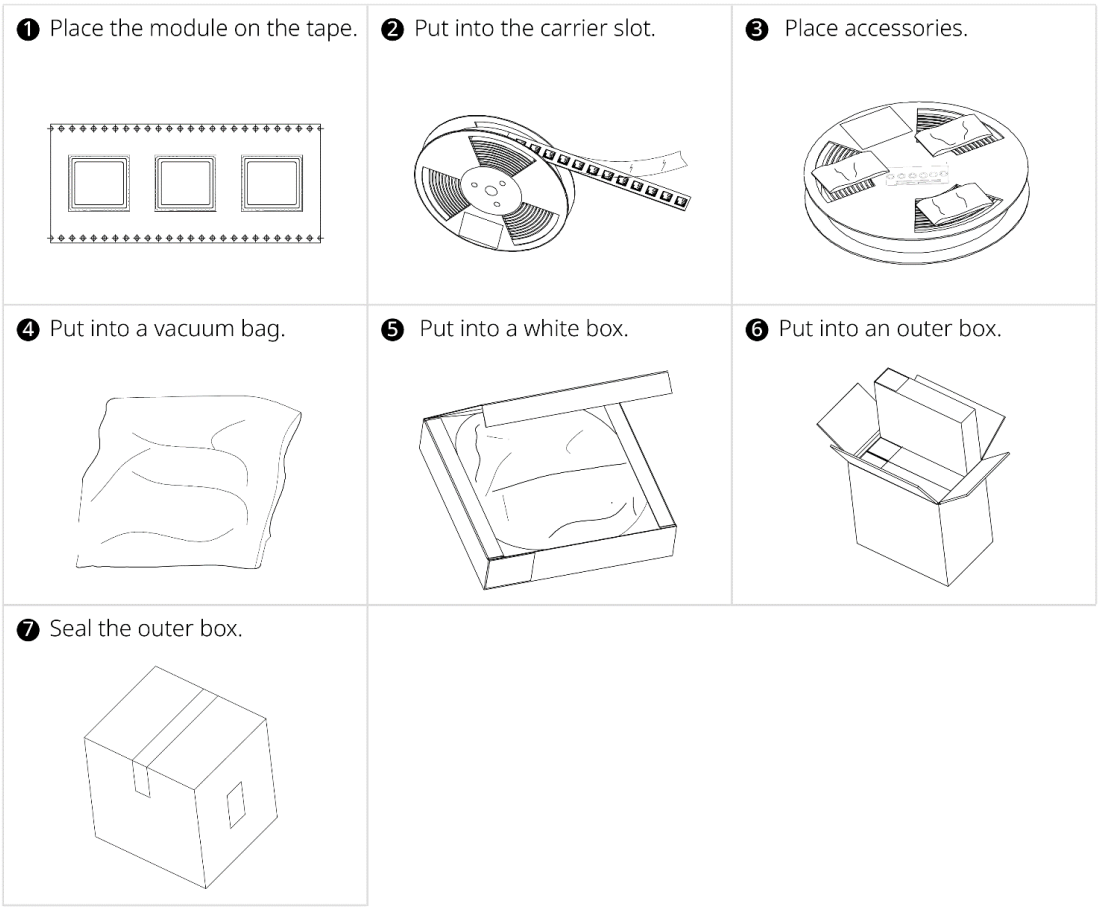


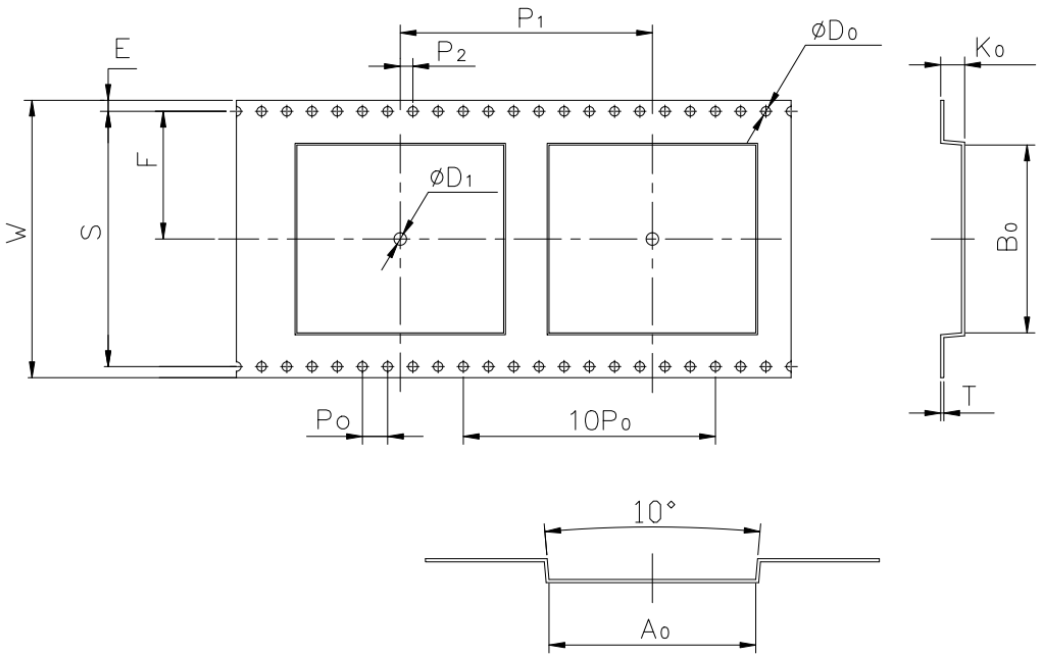

Figure 45. Tape packaging process

1. Place each module into the carrier slot frame in the same direction as specified, and sealing the heat-sealing film.
2. Place the specified number of module tapes as shown in the figure.
3. Before vacuuming, place 3 bags of desiccant and a humidity card above the tape, and paste the label of the carrier tape.
4. Put the whole into a vacuum bag and vacuuming.
5. Put the vacuum electrostatic bag into a white box, only one electrostatic bag is put into a single white box. Buckle the white box and paste the label.
6. Seal the bottom of the outer box, and put the 4 PCS white boxes into the outer box as

shown in the figure.

7. Seal the top of the outer box in an I-shape, paste an outer box label in the rectangular frame on the side, and paste a box sealing label on the top and bottom of the outer box respectively.

## Tape size




| ITEM | A0 | B0 | K0 | P0 | P1 | P2 | T |
|---|---|---|---|---|---|---|---|
| DIM | 32.8±0.1 | 29.8±0.1 | 3.8±0.1 | 4.0±0.1 | 40.0±0.1 | 2.0±0.15 | 0.5±0.05 |
| ITEM | E | F | D0 | D1 | W | 10P0 | S |
| DIM | 1.75±0.1 | 20.2±0.3 | $1.50^{+0.10}_{-0.00}$ | 0.0 | $44.0^{+0.30}_{-0.10}$ | 40.0±0.2 | 40.4±0.1 |

Figure 46. Carrier tape size

## Reel size

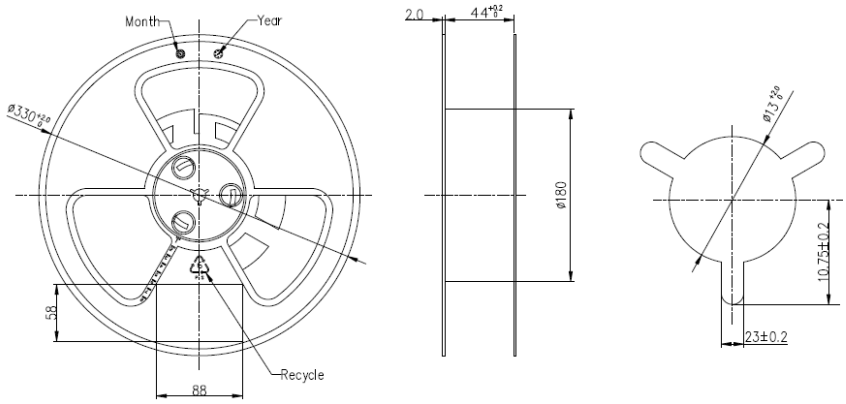



Figure 47. Reel size

Module placement

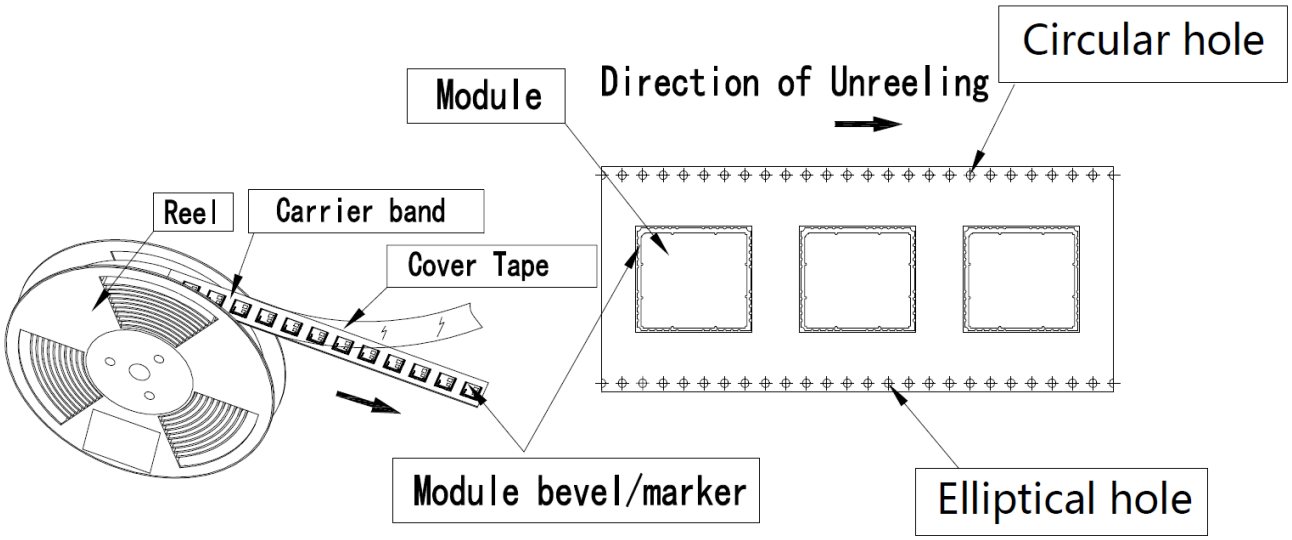



Figure 48. Module placement

# Appendix A Reference Documents

| Category | Document Name |
|---|---|
| Software | *Fibocom_FG132_AT_Commands_User_Manual* |
| Hardware | *Fibocom_FG132_Customer_SCH&PCB_design checklist* |
| | *Fibocom_FG132_Package* |
| | *Fibocom_FG132_3D Module Diagram* |
| | *Fibocom_FG132_Series_Reference_Design* |
| Development kit | *Fibocom_ADP-FG132_Development Board User Guide* |
| | *Fibocom_EVK-LGA-F01_User Guide* |
| Other | *Fibocom_FG132_SMT_Application Design Notes* |
| | *Fibocom_FG132-GL-00_Thermal Design Model* |

# Appendix B Acronyms and Abbreviations

| Acronym and Abbreviation | Description |
|---|---|
| ADC | Analog to Digital Converter |
| ADP | Application Development Platform |
| BT | Bluetooth |
| IPC | IP Camera |
| DCDC | Direct Current to Direct Current |
| DDR | Double Data Rate |
| ESD | Electronic Static Discharge |
| FDD | Frequency Division Duplexing |
| FEM | Front End Module |
| GNSS | Global Navigation Satellite System |
| NR | New Radio |
| LDO | Low Dropout Regulator |
| LTE | Long Term Evolution |
| I2C | Inter Integrated Circuit |
| PCB | Printed Circuit Board |
| PCM | Pulse Code Modulation |
| PMU | Power Manager Unit |
| RF | Radio Frequency |
| RTC | Real Time Clock |
| SGMII | Serial Gigabit Media Independent Interface |
| SIM | Subscriber Identification Module |
| SPI | Serial Peripheral Interface |
| TDD | Time Division Duplexing |
| UART | Universal Asynchronous Receiver Transmitter |
| USB | Universal Serial Bus |
| WLAN | Wireless Local Area Network |